Process-to-System Level Study of Low-Voltage Thin Film Transistors: Fabrication, Modeling, and Simulation

Thesis submitted in partial fulfillment

for the Award of Degree of

Doctor of Philosophy

By

Mukuljeet Singh Mehrolia

RAJIV GANDHI INSTITUTE OF PETROLEUM TECHNOLOGY

JAIS, 229304

21EE0102 ***2025***

CERTIFICATE

It is certified that the work contained in the thesis titled ***Process-to-System Level Study of Low-Voltage Thin Film Transistors: Fabrication, Modeling, and Simulation*** by ***Mukuljeet Singh Mehrolia*** has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

It is further certified that the student has fulfilled all the requirements of Comprehensive, Candidacy, and Open Seminar.

Dr. Abhishek Kumar Singh

(Thesis Supervisor)

DECLARATION BY THE CANDIDATE

I, ***Mukuljeet Singh Mehrolia***, certify that the work embodied in this thesis is my own bonafide work and carried out by me under the supervision of *Dr. Abhishek Kumar Singh* from *January 2022* to *June 2025,* at the *Department of Electrical and Electronics Engineering,* Rajiv Gandhi Institute of Petroleum Technology, Jais. The matter embodied in this thesis has not been submitted for the award of any other degree. I declare that I have faithfully acknowledged and given credits to the research workers wherever their works have been cited in my work in this thesis. I further declare that I have not willfully copied any other's work, paragraphs, text, data, results, etc., reported in journals, books, magazines, reports dissertations, theses, etc., or available at websites and have not included them in this thesis and have not cited as my own work.

Date:

Place: Jais, Amethi **Mukuljeet Singh Mehrolia**

CERTIFICATE BY THE SUPERVISOR

It is certified that the above statement made by the student is correct to the best of my knowledge.

Dr. Abhishek Kumar Singh

(Thesis Supervisor)

Head of the Department

CERTIFICATE

CERTIFIED that the work contained in the thesis titled ***Process-to-System Level Study of Low-Voltage Thin Film Transistors: Fabrication, Modeling, and Simulation*** by ***Mr. Mukuljeet Singh Mehrolia*** has been carried out under my supervision. It is also certified that he fulfilled the mandatory requirement of TWO quality publications that arose out of his thesis work.

It is further certified that the two publications (copies enclosed) of the aforesaid ***Mr. Mukuljeet Singh Mehrolia*** have been published in the Journals indexed by –

(a) SCI

(b) SCI Extended

(c) SCOPUS

Dr. Abhishek Kumar Singh **Dr. Saurabh Pandey**

(Thesis Supervisor) (Convener, DPGC)

COPYRIGHT TRANSFER CERTIFICATE

Title of the Thesis: ***Process-to-System Level Study of Low-Voltage Thin Film Transistors: Fabrication, Modeling, and Simulation***

Name of the Student: ***Mukuljeet Singh Mehrolia***

Copyright Transfer

The undersigned hereby assigns to the Rajiv Gandhi Institute of Petroleum Technology Jais all rights under copyright that may exist in and for the above thesis submitted for the award of the "Doctor of Philosophy".

Date:
Place: Jais, Amethi **Mukuljeet Singh Mehrolia**

Note: However, the author may reproduce or authorize others to reproduce material extracted verbatim from the thesis or derivative of the thesis for the author's personal use provided that the source and the Institute's copyright notice are indicated.

ACKNOWLEDGEMENT

First, I offer my respectful and humble obeisances unto my spiritual masters, His Holiness Bhakti Dhira Damodara Swami Maharaja, His Holiness Bhakti Tirth Swami Maharaja, and His Divine Grace A.C. Bhaktivedanta Swami Srila Prabhupada, for their countless blessings, wishes, and divine grace unto me, which motivated and inspired me a lot to work hard for completing my PhD degree. Along with this, I am very grateful and thankful to my thesis supervisor, Dr. Abhishek Kumar Singh, for his constant support, guidance, valuable advice and suggestions, and freedom of discussion throughout the entire duration of the research work. Especially his wonderful presentation skills and explaining the technical content to the audience in an easy way remain a crucial factor of motivation for me.

I also express my gratefulness and thankfulness to my family members, friends, seniors and well-wishers for their wonderful wishes, sacrifices, and unconditional love, which has always been supportive for completing this doctoral program.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS/NOTATIONS

AFM	Atomic Force Microscopy	PBTTT-C14	Poly[2,5-bis(3-tetradecylthiophen-2-yl) thieno[3,2-b] thiophene]
OTFT	Organic Thin Film Transistor	PET	Poly (ethylene terephthalate)
TFT	Thin Film Transistor	PEN	Polyethylene naphthalate
FET	Field Effect Transistor	Ppm	Parts per million
FTM	Floating Film Transfer method	Ppb	Parts per billion
OSC	Organic Semiconductor	TFT	Thin Film Transistor
C-f	Capacitance-frequency curve	a-IGZO	Amorphous Indium Gallium Zinc Oxide
LoD	Limit of Detection	I_{DS}	Drain-source current
ITO	Indium Tin Oxide	V_{DS}	Drain-source voltage
PBS	Positive Bias Stress	V_{GS}	Gate-source voltage
HOMO	Highest Occupied Molecular Orbital	E_F	Fermi Energy Level
LUMO	Lowest Unoccupied Molecular Orbital	E_g	Energy Bandgap
CMOS	Complementary Metal Oxide Semiconductor	C_{OX}	Oxide Capacitance
H_2S	Hydrogen Sulphide	W	Channel Width
HMDS	Hexamethyldisilazane	L	Channel Length
IC	Integrated Circuit	V_{TH}	Threshold Voltage
DOS	Density of States	SS	Subthreshold Swing
TAOS	Transparent Amorphous Oxide Semiconductor	S	Gas Sensing Response
ALU	Arithmetic Logic Unit	N_T	Total Trap Density
TCAD	Technology Computer-Aided Design	μ	Mobility
DI	Deionized Water	t_{ox}	Oxide Thickness
LCAO	Linear Combination of Atomic Orbitals	ΔV_{TH}	Change in Threshold Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor	$T_{channel}$	Channel Thickness

PREFACE

Recently, thin-film transistors (TFTs) have garnered significant attention from researchers due to their wide range of applications, including electronics, gas sensing, memory circuits, medical devices, and optoelectronics. Advancements in deposition techniques have proven highly effective in developing cost-effective, solution-processed, low-voltage TFTs that meet the requirements of various applications. Based on the type of semiconductor used, TFTs are classified as either organic thin-film transistors (OTFTs) or inorganic thin-film transistors. Both have their unique advantages: OTFTs are preferred for flexible applications, such as flexible LEDs, memories, and sensors, whereas inorganic thin-film transistors are commonly used for transparent and optical applications. The investigations reveal that the requirements of low-power applications can be met by utilizing low-voltage TFTs operating at 1–2 V with high-k dielectric materials such as $SrZrO_x$, HfO_2, etc. Furthermore, by using organic semiconductors, solution-processed, cost-effective, low-voltage, flexible, and silicon substrate-based OTFTs can be fabricated for gas sensing and electronic applications. The Silvaco-Techmodeler and Silvaco-Gateway tools have been employed to realize various complex analog and digital circuits. This thesis focuses on the fabrication and simulation of low-voltage TFTs for sensing and electronic applications.

Chapter 1 of this thesis explains the background and advancements related to TFT devices, different types of TFT architecture and configuration depending upon semiconductor and dielectric materials, the fundamental and working operation of TFT devices, various techniques employed for thin film deposition, the history and introduction related to compact modeling of TFT devices and the role of compact modeling in the

realization of analog and digital, different stages involved for compact modeling of TFT devices using the Silvaco-Techmodeler tool, and applications of TFT devices.

Chapter 2 of this thesis explains the fabrication of Ag-doped PBTTT-C14 (poly[2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene]) based OTFT developed on silicon substrate, and $SrZrO_x$ is used as a high-k dielectric, which led to a low voltage of 1.5 V. The floating film transfer method (FTM) has been used for film deposition as it is cost-effective in nature with minimal wastage of chemicals. Film characterization of semiconductor and dielectric layers ensures smooth films free from trap charges. This Ag-doped PBTTT-C14-based OTFT on a silicon substrate has been used for the sensing of H_2S gas, which gives the sensing response higher than 80% and a limit of detection (LoD) of ~15.17 ppb.

Chapter 3 explains the fabrication of the PBTTT-C14 based OTFT device established over a flexible PET (Polyethylene terephthalate) substrate, and the composition of PMMA (Polymethyl methacrylate) and $SrZrO_X$ in 20:80 is taken to be utilized as a high-k dielectric material. This PBTTT-C14 based OTFT device operated at a low voltage of 1 V. The film of PBTTT-C14 has been deposited by means of the FTM technique. Active layer and dielectric film characterization is performed along with this bandgap. Capacitance-frequency and leakage current density of the dielectric layer are also estimated. This fabricated flexible OTFT device is compact modeled using the Silvaco-Techmodeler tool. The experimental data and modeled data completely superimpose on each other, assuring a small fraction of error of less than 1 %. This compact, modeled, flexible OTFT is used for the implementation of an inverter circuit over the Silvaco-Gateway platform and exhibits a high gain of 39.77 and a small propagation delay (τ_{PD}) of 35 ns.

Chapter 4 explains the simulation of an inorganic semiconductor, an amorphous indium gallium zinc oxide (a-IGZO)-based low-voltage TFT, using the Silvaco-Atlas tool, followed by an analysis of the device characteristics. This chapter describes the materials used for the electrodes (PET for all electrodes), gate oxide (HfO_2), and semiconductor in the simulation of a fully transparent, flexible, low-voltage thin-film transistor. The device characteristics confirm that the fully transparent TFT operates at an operating voltage of 2 V. Furthermore, this device is compact modeled using the Silvaco-Techmodeler tool, and using this compact, flexible, transparent, and low-voltage model, full adder and full subtractor circuits are simulated using the Silvaco-Gateway tool, and with the help of transient analysis, respective truth tables are verified.

In ***Chapter 5***, compact modeling and circuit simulation using Silvaco-Techmodeler and Silvaco Gateway tools are explained in a detailed manner, and all the steps are elaborated for ease of understanding . The devices fabricated and simulated in the previous chapters are compact modeled, demonstrating perfect matching and superimposition of curves between the modeled data and the simulated or fabricated data, with a small margin of error (less than 1%). Additionally, diagrams and graphs are provided to support the content. This model is subsequently imported for circuit simulation. The Silvaco-Gateway tool is used to implement circuits utilizing the compact modeled devices. Circuits such as inverters, full adders, full subtractors, half adders, logic gate families, 1-bit magnitude comparators, and 4:1 multiplexer are implemented. The respective truth tables, transient characteristics, and voltage transfer characteristics are verified. Based on these characteristics, parameters such as voltage gain and propagation delay are evaluated. The working of the Silvaco-Gateway tool is explained in detail. Additionally, a brief user guide

is provided, describing how to use the Silvaco-Techmodeler and Silvaco-Gateway tools effectively.

In ***Chapter 6***, the stability analysis of a-IGZO-based low-voltage TFTs is performed. The device has been simulated by means of the Silvaco-Atlas tool. Factors such as the thickness of the semiconductor layer (10/20/30 nm), the thickness of the dielectric layer (70/60/50/40 nm), and the semiconductor-interface properties, which impact the device performance parameters, are observed, and the change in threshold voltage $\Delta V_{TH} = V_{TH}$ ("off-on state") $- V_{TH}$ ("on-off state") is analysed and discussed. Graphs are provided to support and illustrate all the results.

In ***Chapter 7***, a summary of all the case studies, work, and overall conclusions is presented, along with the future scope of the thesis.

Chapter 1

Introduction

1.1 Background and Past History of Thin Film Transistors

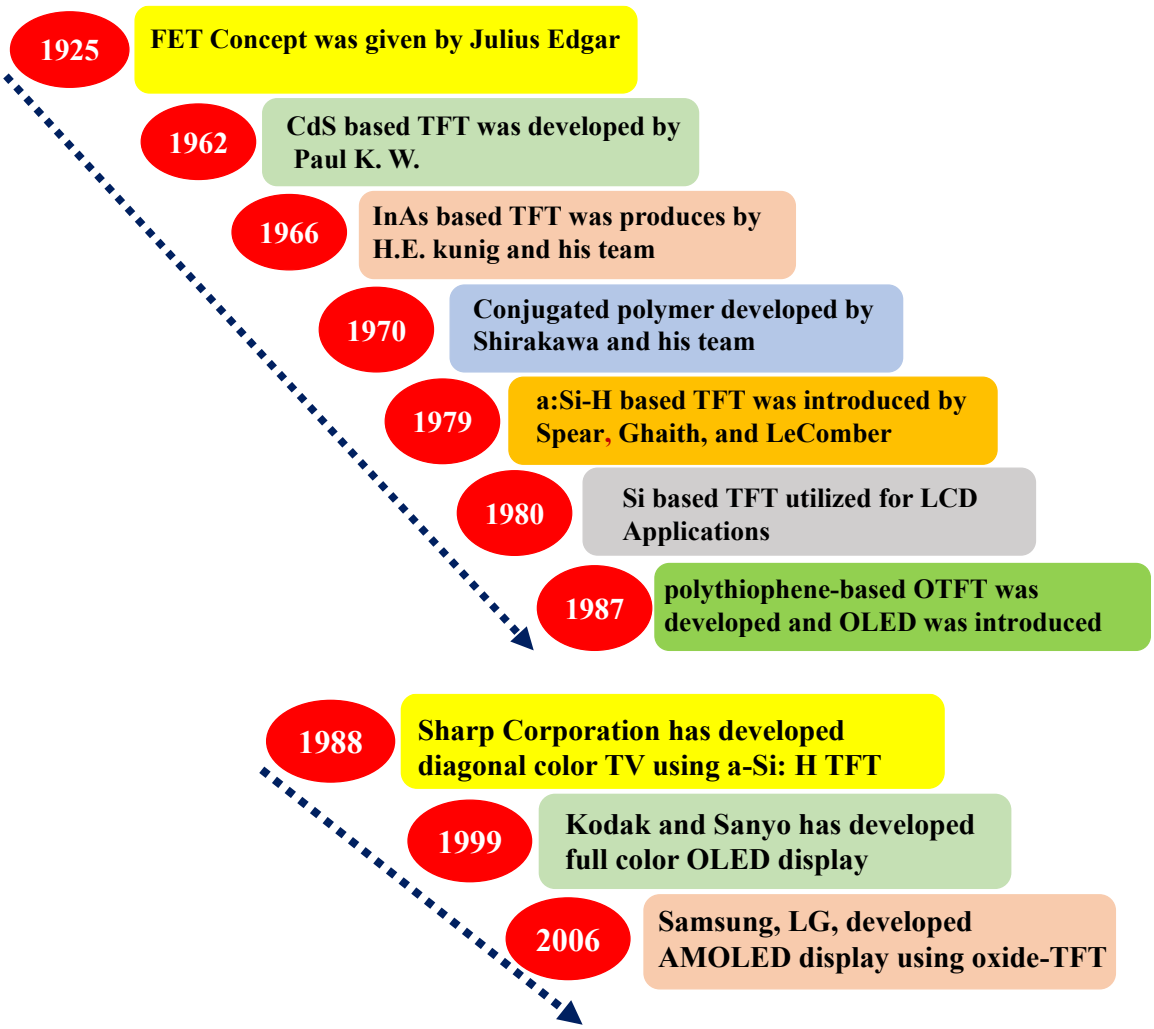


Figure 1.1 Journey of advancement in the field of transistor from FET to TFT.

1.2 Period of Inorganic Thin Film Transistor

In 1925, Julius Edgar Lilienfeld first proposed the concept of the field-effect transistor (FET). While the metal-oxide-semiconductor FET (MOSFET) garnered significant attention from researchers, its fabrication process was considered highly complex and

expensive, posing substantial challenges to researchers attempting to develop this device. To address these issues, alternative technologies to MOSFETs were explored [1].In 1962, the first thin-film transistor (TFT) was fabricated by Paul K. Weimer, using cadmium sulfide (CdS) as the active material [2]. Subsequently, in 1966, indium arsenide (InAs)-based TFTs were developed by H.E. Kunig and T.P. Brody. These TFTs operated in both enhancement and depletion modes [3]. During the 1970s, a basic TFT device was developed, offering a cost-effective solution for applications in memory circuits, display circuits, sensors, and other areas.In 1970, Shirakawa and his group of researchers successfully developed a conjugated polymer and demonstrated its doping capability for the first time [4]. However, constraints such as low charge carrier mobility limited the performance of organic electronics. This led to further advancements and growth in fields such as flexible electronics and organic electronics [5]. In 1979, Spear, Ghaith, and LeComber introduced a TFT device based on hydrogenated amorphous silicon (a-Si:H). This a-Si:H TFT exhibited enhanced mobility and excellent performance, marking a significant milestone in the development of active-matrix liquid crystal display (LCD) panels for commercial production in Japan [1]. The same year, W.E. Spear and his team developed a TFT with amorphous silicon (a-Si) as the active layer. This innovation further enhanced mobility and performance, solidifying the foundation for the use of TFTs in LCDs [6]. In the 1980s, TFT devices utilizing silicon as the active layer gained widespread preference due to their high potential for liquid crystal display (LCD) applications [7], [8]. In 1987, polythiophene-based organic thin-film transistors (OTFTs) were developed, offering higher conductivity. The same year, Ching W. Tang and his group introduced organic light-emitting diodes (OLEDs) for the first time [9].In 1988, under the guidance of T. Nagayasu, Sharp Corporation utilized a-Si:H-based TFTs to develop a 14-inch diagonal flat-panel color television [10]. This development marked a

crucial moment in the electronics industry, demonstrating the potential of LCDs as a substitute for cathode-ray tube (CRT) displays.Building on the advancements in inorganic TFTs for display applications, Kodak and Sanyo introduced a full-color active-matrix OLED display in 1999. This 2.4-inch organic-based display was a significant milestone, highlighting the utility and versatility of OLED technology in modern electronics [11]. The middle of 1990, from the production point of view, Korean and Japanese companies played in crucial role for the AMLCD in high-scale production. At the same time, to fulfill the requirement of semiconductor device exhibiting high magnitude mobility employed for TFT large amount of hard work were done by researchers [12]. Nearly around 1990, the hard work of researchers pay-off a developed TFT having poly-Si (LTPS) [low temperature polycrystalline silicon] as semiconductor exhibiting excellent features as low processing temperature (< 600 ℃), polycrystalline nature, high on-off ratio ~ 10^{10} and electron mobility (μ_n) ~ 35 cm^2/V-sec [13]. In addition to this, this decade also witnesses different deposition techniques adopted by researchers such physical vapor deposition (PVD) for the development of TFT, these such techniques lead to progress and growth in field of TFT at that duration [14]. Along with this, to further carry forward to develop device which requires low-processing temperature, to meet this goal research and engineering is done in the material properties. Certain attempts, crystallization has been opted to transform LTPS into a-Si: H. To perform crystallization techniques such as laser annealing, non-crystallization, excimer-laser annealing, etc. methods are used [15], [16].

1.3 Period of Oxide Thin Film Transistor

In 1960, oxide material based TFT was introduced but further research and investigation was not done. Later on, it has found that oxide based TFT device posses property such as enhanced switching speed and higher magnitude of mobility. In 1964-68, SnO_2 and ZnO based TFT was developed [17], [18]. After the long duration of more than 3 decades, H.

Hosono and the group of researchers has utilized oxide material for the development of active-matrix organic light-emitting diode (AMOLED) [19]. Followed by J. F. Wager, E. M. C. Fortunato's and their respective teams have done so much research work in this field of oxide material based TFT which seems benefits to academics and industrial domains [20], [21]. In comparison to a-Si: H and LTPS, oxide material-based device provides enhanced mobility, transparent nature, deposition temperature is low, stable device parameters, etc. Some famous oxide materials are zinc oxide (ZnO), indium gallium zinc oxide (In-Ga-Zn-O), tin oxide (SnO_2), indium oxide (In_2O_3), zinc-tin oxide (Zn-Sn-O (ZTO)), gallium-tin-zinc oxide alloy (Ga-Sn-Zn-O (GSZO)), zinc-indium oxide (Zn-In-O (ZIO)), titanium oxide (TiO_2), indium zinc oxide (In-Zn-O (IZO)), indium gallium oxide (In-Ga-O), etc [22], [23]. In 2006, highly recognized companies as Samsung, Sharp, LG, etc. has established AMOLED display with the help of oxide TFTs [24].

1.4 Period of Organic Thin Film Transistor

The introduction of conducting organic polymers into family of semiconductor materials have gathered the high attentions of researchers due to there utilization of different types of optoelectronics and electronics devices. In comparison to inorganic semiconductor, the development of organic semiconductor is cost-effective in nature and involves non-complex techniques for its fabrication [25]. Organic semiconductors are classified into two categories as small molecules and conjugated polymers [26]. Around 1960, research work in the domain of organic molecules e.g. anthracene, etc. which states its ground-state and excited-state electronic structure [5]. In continuation to this, in 1970 Shirakawa and the group of researchers have developed doping governed semiconductor polymers, this efforts, hard work and research of these researchers led a push to the research community to further examine on these materials. This push resulted very fruitful as

Shirakawa and his team has founded and established conducting polymer which was highly appreciated and honored by Nobel Prize in 2000. The introduction of organic semiconductor seems very helpful for different applications such as dry photocopying also termed as xerography, which had gathered high recognitions of user during 1980's [5], [27]. In the upcoming decades, further exploration and research is done in this organic semiconductor and developed several types of devices as electrochemical cells, solar cells, organic light-emitting diodes (OLEDs), organic memories, xerography, organic field-effect transistors (OFETs), printed organic circuits, organic photodetectors, and organic biosensors [28], [29]. From the starting period, it is quite-clear that the molecular order is completely associated with the charge carrier mobility exist in the material which is used as semiconductor film in organic thin film transistor (OTFT). At the beginning stage, pentacene is used by researchers to develop OTFT [30] and later these OTFT's are further classified and explored for several electronics applications. In 2004, for the first time ambipolar light emitting transistor (LET) was founded, this type of transistor posses' properties such as switching and optoelectronics at the same time [31], [32]. Substrates as flexible/ transparent/ plastic are used for the feasible fabrication of OTFT, OFET has opened the opportunity for the further utilization in the field of flexible electronics [31]. The need and requirement of users for electronic and optoelectronics device which is cost-effective in nature is resolved and fulfilled by organic electronics. Some constraints and issues exist with organic semiconductors materials such as charge-carrier mobility and stability issues. In upcoming years, an attempt had tried to eliminate these mobility and stability challenge by developing Oligofluorene derivatives-based materials based OTFT devices [33]. The target of higher magnitude mobility was also solved by Bell Laboratory in 2005 by developing OFET device where role of organic semiconductor is played by organic selenium (1-2,6- diphenylbenzo[1,2-b:4,5b0] diselenophene (DPh-

BDSe) [34]. These large variety applications of OTFT have gathered the high attention of industries for commercial application circuits as high-speed display driver circuit, organic memories, sensors, etc. Newly, organic semiconductor 2,6-diphenylanthracene (DPA) based OTFT was developed which exhibits higher magnitude of mobility ~ 34 cm^2/V-s that can used for optoelectronics devices [35]. Researchers are working very hardly on the stability analysis of organic materials which would be beneficial from ecological point of view. Similarly, 2,7-dioctyl benzathine benzothiophene (C8-BTBT) based OTFT device exhibits average mobility of 17 cm^2/V-s which is in similar range of the inorganic semiconductor based TFTs [36]–[40]. These OTFT devices exhibiting higher magnitude of mobility raised high demand for various applications e.g. floating gate flash memories, etc [40]–[42]. Pentacene based OTFT device in which SiO_2 acted as gate dielectric and Cu is served as source/ drain contact and having the on-off ratio of 10^4 has been previously reported by researchers. In Pentacene based memories it has been noticed that light absorption highly impact on the memory window in which hole-trapping dominate electron-trapping in it [43]. It is well known that Organic semiconductor possess light emission characteristics, researchers worked in past years has developed OLEDs offer superior quantum efficiency. The development of organic light-emitting field-effect transistor (OLET) proclaim that organic semiconductors are compatible for the application of optoelectronic devices [44]. All the research work done in the domain of organic semiconductor mentioned above states work, investigate and study more in this field to establish OTFT device for different applications as gas sensing, flexible electronics, etc.

1.5 Organic Semiconductors and Charge Transportation Mechanism

Organic semiconductor is divided into two major categories namely (1) small molecules and (2) polymers. Some limitations exist with polymers for its dispersion in certain

solvents like in polar solvent (e.g. H_2O, alcohol) due to non-polar nature of π- conjugated small molecule. Similarly for the non-polar organic solvents (e.g. benzene, toluene, octane and hexane) due to unbearable π- conjugated structure and lacking the existence of hydrophobic group as -CH_3. The solubility can become possible by the addition of long chain aliphatic group. Small molecules and polymers are further categorized [45]–[48] in **Figure 1.2**.

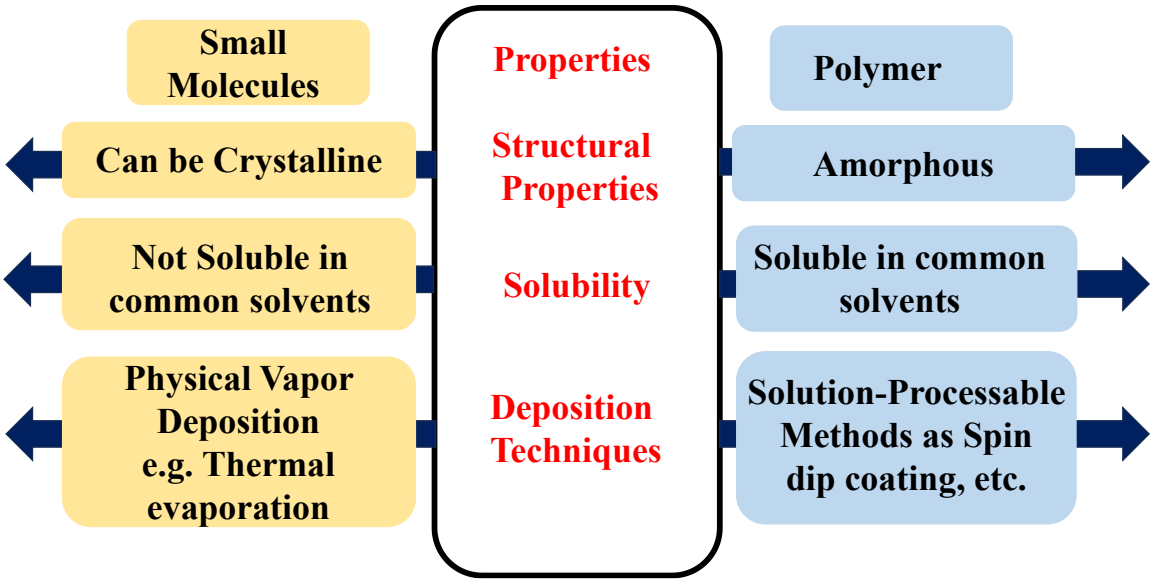


Figure 1.2 Distinguishes between Small molecules and Polymers.

Although, researchers have done high research in the domain of organic-semiconductors since last 30-40 years, one topic still exists which arises many questions and debatable between the researchers that is transportation of charge-carrier of organic material [46]. This section, charge transport phenomenon is elaborated by the means associated physics and models [49]. Organic semiconductor belongs to the family of molecular system. Hence, using molecular orbital theory this charge transportation phenomenon is elaborated [50]. This model states that, two atoms possessing equivalent energy are come in contact with each other having very close-range results into splitting of energy levels and lead to generation two distinct molecular energy levels in which one exhibits reduced

energy level in comparison to original one and other offered enhanced energy level. In most of the molecules, absolute calculation is not made possible by the recently formed molecular orbitals. Hence, to fulfill this objective an estimation named as Linear Combination of Atomic Orbitals (LCAO) is used. As stated in this LCAO theory, the overlapping of the atomic orbitals leads to formation of molecular orbitals (MOs). The combination of atomic orbitals being linear in nature led to the estimation of molecular orbitals (LCAO-MO) [51].

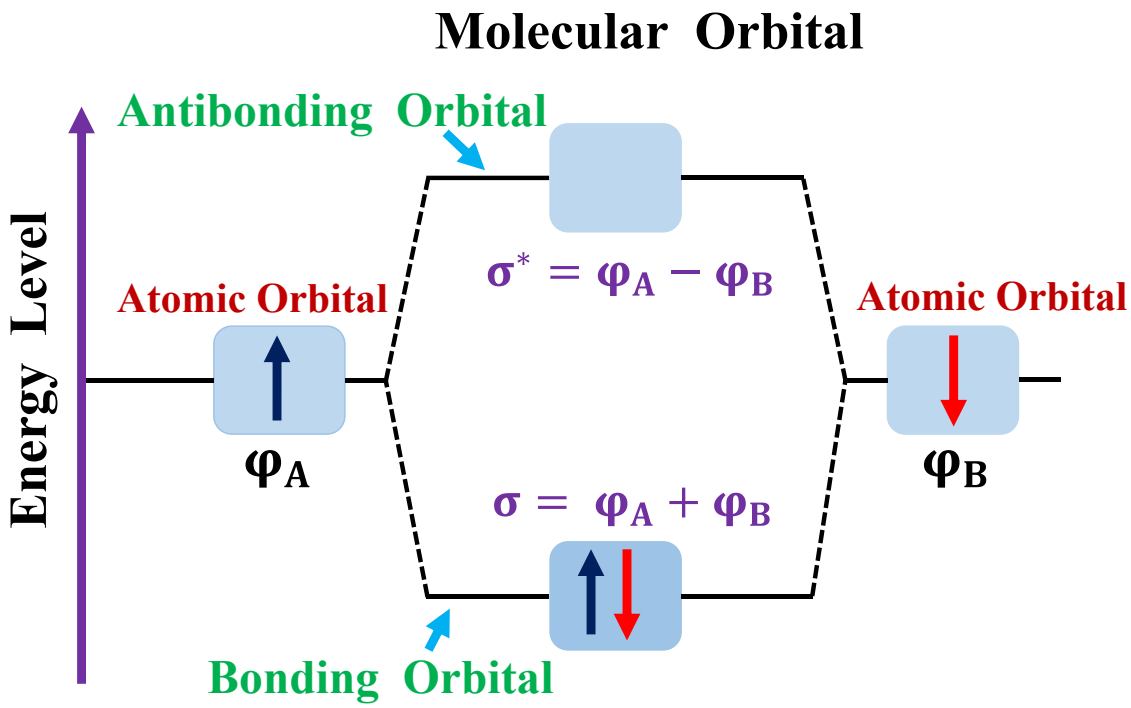


Figure 1.3 Antibonding and Bonding orbitals creation for diatomic hydrogen molecule.

Hence, for diatomic molecule, the wave functions of these atomic orbitals for these two atoms named as A and B are refereed as φ_A and φ_B which resulted into creating molecular orbital (φ_M) as mentioned by LCAO theory, (φ_M) is expressed in the following equations:

$$\varphi_M = \varphi_A \pm \varphi_B \qquad (1.1)$$

The overlapping of two atomic orbitals resulting in the creation of bonding (σ) and antibonding (σ^*) molecular orbitals respectively, these bonding (σ) and antibonding (σ^*) molecular orbitals are the mathematical related to the addition and subtraction wave functions that are shown in equations (1.2) and (1.3).

$$(\sigma) = \varphi_A + \varphi_B \qquad (1.2)$$

$$(\sigma^*) = \varphi_A - \varphi_B \qquad (1.3)$$

Generally, constructive interference occurs in which two electron waves strengthen each other leads to establish (σ) molecular orbital, whereas in destructive interference where both waves nullify each other forms (σ^*) antibonding molecular orbital. This is shown in **Figure 1.3**.

Molecular orbitals are further categories into two classes that are 1. Sigma (σ) and 2. Pi (π) bond. The organic semiconductor has conjugated π electronic system in which single bond and double bond are arranged in alternative manner. For the estimation of bandgap of organic semiconductor material this theory of molecular orbitals having bonding and antibonding plays a crucial role. In organic semiconductor, the charge carriers are excited from bonding molecular orbital to antibonding molecular orbital of the conjugated electron system. The LUMO bonding (Lowest unoccupied molecular orbital) of organic semiconductor is demonstrated by the antibonding π*-orbital and HOMO bonding (Highest Occupied molecular orbital) is displayed by bonding π-orbital. The gap of energy between HOMO and LUMO states the bandgap of organic semiconductor. This is well explained in **Figure 1.4**. In the thesis, the interest of research in which we worked is organic polymer semiconductor as process is feasible at low-temperature and availability of π- conjugated bond. The conjugated polymer is formed because of the hybridized

nature of “C” atoms which led to “π” bonded electron delocalization with the C atoms resides nearby.

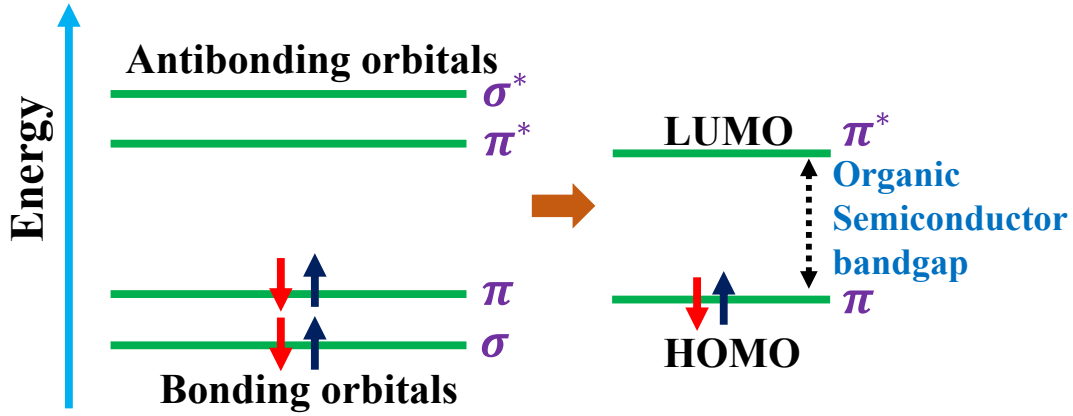


Figure 1.4 Bandgap of Organic semiconductor in terms of energy level of π conjugated molecule.

1.6 Merits and Demerits of Inorganic and Organic Semiconductors

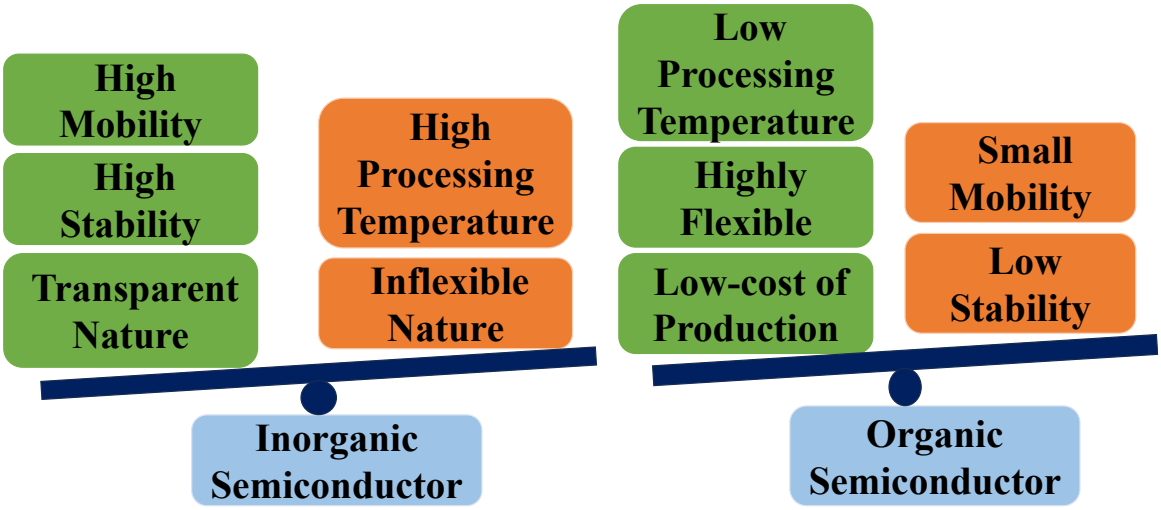


Figure 1.5 States the advantages and disadvantages of Inorganic and Organic Semiconductor.

A qualitative analysis has performed in which the merits and demerits of organic and inorganic semiconductors are explained [52]. Organic semiconductors offer several features as low-processing temperature, low-cost of production, flexible nature but in

terms of mobility and stability inorganic semiconductors dominates organic devices [53]. In **Figure 1.5**, for different parameters a comparison analysis is performed among both inorganic and organic semiconductor is performed.

1.7 Working Mechanisms of Thin Film Transistors

Thin film transistor belongs to the class of MOSFET, the working principle is similar to MOSFETs but the fabrication of TFT device is feasible on any types of substrates [5], [52], [54].

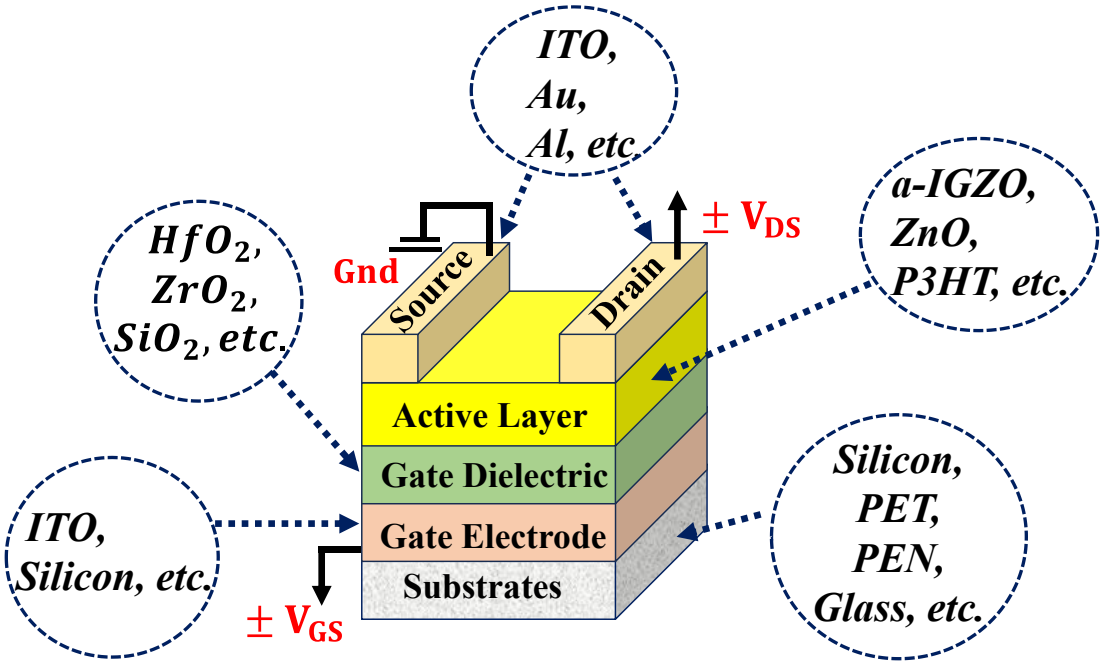


Figure 1.6 Showing the schematic of TFT and materials associated with different layer.

In a-Si TFT in which active layer is amorphous silicon is developed with the help of PECVD technique which may posses' large numbers of defects in comparison to single-crystalline Silicon which can act as an obstacle for charge-carrier transportation and impact on mobility of TFT. Along with this, several structures exist which are appropriate for high-speed applications, space applications, etc. these structures are named as silicon on sapphire (SOS), silicon on insulator (SOI) and silicon on zirconia (SOZ) [55], [56].

These structures offer various features in comparison to MOSFETs such as good isolation to diminish magnitude of capacitance to the substrate and refines the subthreshold swing. In SOI type structure certain issues exist as costly wafer, kink effect which seem a disadvantage for this structure [57]. In the upcoming sections the steps involved in the fabrication of TFT device, region of operation and device characteristics are explained.

TFT is divided into three-parts (1) active layer of semiconductor material (2) dielectric layer of insulator material (3) electrodes for gate, drain and source. In **Figure 1.6** all these layers and electrodes are shown.

For developing metal-semiconductor contact, both source and drain electrodes are developed on the active layer i.e. channel of the TFT, whereas the gate electrode kept separated from active layer with the help of dielectric layer. This dielectric layer is inserted in the middle of gate electrode and active layer of semiconductor material resulting in developing non-direct linkage among these two regions [13], [23], [55]. Among source and drain electrodes, semiconductor material is situated [22], [23]. The target of device is to govern drain current (I_{DS}) with the help of gate-source voltage that can be attained when semiconductor-dielectric interface is accumulated by charge carriers. One of the unique features of TFT device is that it offers high flexibility for structures which helps the researchers for all types of possible fabrication. Additionally, TFT is further divided in 4 different groups on the basis of active layer place, which is displayed in **Figure 1.7**. The place of electrodes as gate, drain and source decide configuration of TFT structure either staggered or coplanar. When all the electrodes (source, drain and gate) lie on the same view of active layer it is terms coplanar TFT structure otherwise it is stated as staggered TFT structure. Similarly, according to the place of gate electrode, TFT structure can be further classified as top gate or bottom gate.

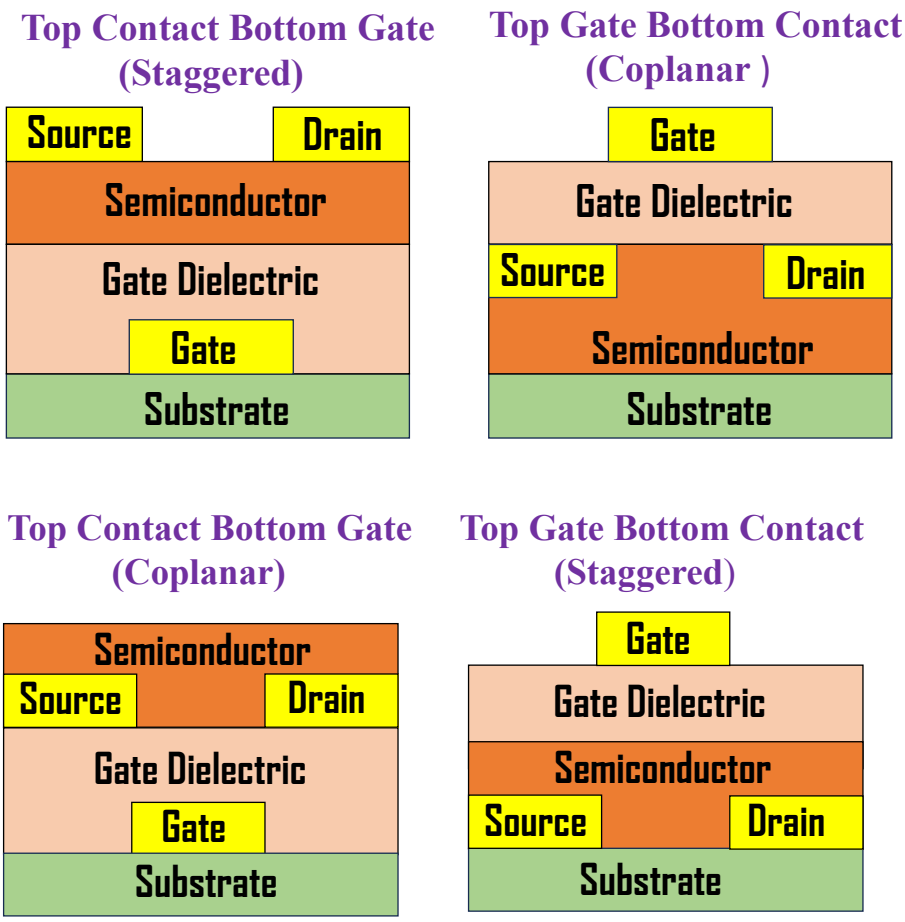


Figure 1.7 Stating Different configurations of TFT structures.

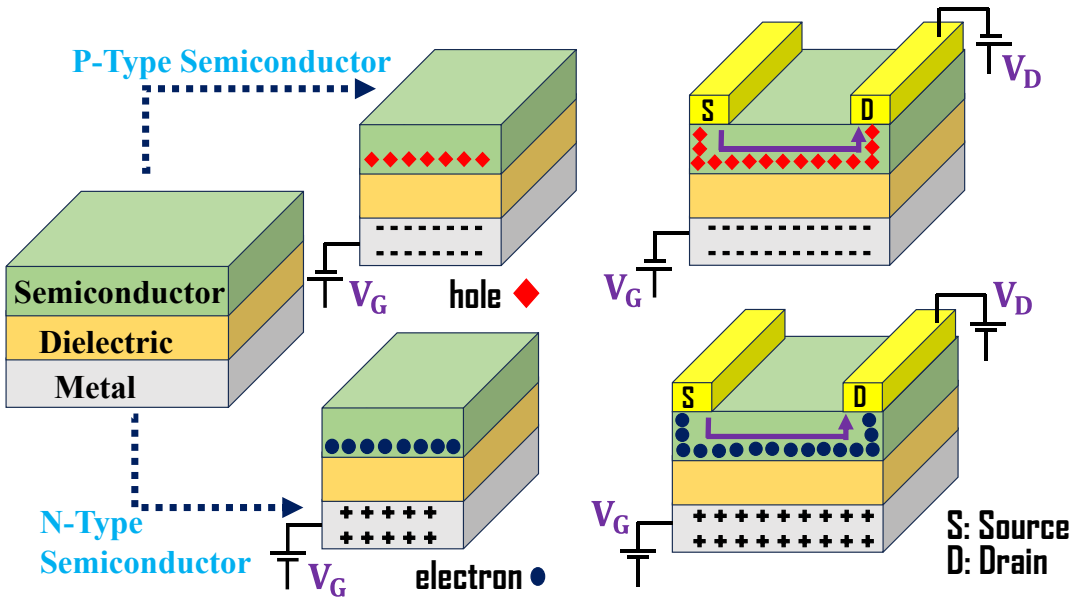


Figure 1.8 Showing the operation of N-TFT and P-TFT when they are subjected to biasing.

In MOSFET, gate voltage governs the device in the same way it also controls the TFT device. The working of MOS (m-metal, oxide-insulator, s-semiconductor) structure is explained in **Figure 1.8**, when voltage biasing is supplied to the metal plate, the same charge is seeming over metal plate which is conductive in nature. At the semiconductor-insulator, reverse type of charge are emerged i.e. electron would gather when negative supply is there or holes would be there when positive supply is there. The collection of charge carrier at the interface led to produce a channel for the conduction operation which is displayed in **Figure 1.8**. The charge density (Q) of the channel is directly associated with the voltage (V) supplied to the metal plate [55]. This charge density is regulated by two factors as applied gate voltage and capacitance. C is capacitance lies within metal and semiconductor region. Dielectric capacitance is expressed as $^{\varepsilon_r . \mathrm{A}}/_{t_{OX}}$ where ε_r is dielectric constant which varies material to material and t_{OX} is oxide thickness. Hence, the higher magnitude of oxide capacitance can be obtained by the employment of high-k dielectric material or by lowering the oxide thickness.

The region of operation of TFT is accumulation region whereas, for MOSFET the region is inversion [55]. For a n-channel TFT, electrons are the majority charge carrier whose concentration ($\mathrm{n_n}$) is which is function of energy difference. Similarly, for p-channel TFT, holes are majority charge carrier whose concentration ($\mathrm{p_p}$), both the carrier concentration are expressed in following equations (1.4 and 1.5) [55].

$$\mathrm{n_n} = \mathrm{n_i}\, \mathrm{e}^{\{\mathrm{E_{fn}} - \mathrm{E_i}\}/\mathrm{kT}} \quad (1.4)$$

$$\mathrm{p_p} = \mathrm{n_i}\, \mathrm{e}^{\{\mathrm{E_i} - \mathrm{E_{fp}}\}/\mathrm{kT}} \quad (1.5)$$

When positive voltage is supplied to the “N-TFT”, the energy band tends to move in the downward direction because at the interface of insulator-semiconductor channel the

electron concentration got enhanced in comparison to the initial condition case when no biasing is applied. This phenomenon is termed as accumulation mode. In the same manner, for "P-TFT" the energy band would move towards the upwards direction because the hole concentration got incremented over the interface surface. This accumulation mode of operation is shown in **Figure 1.9.**

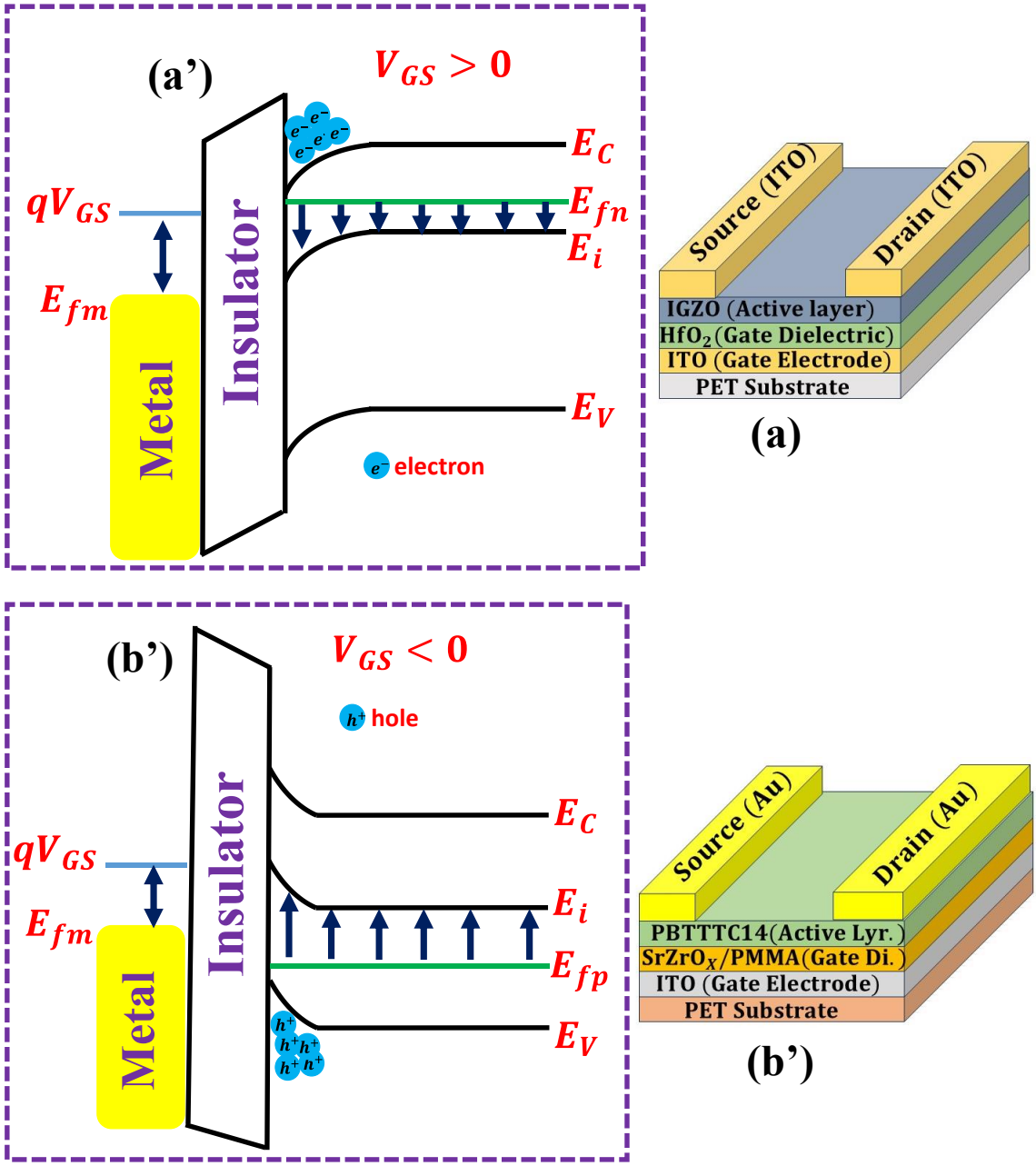


Figure 1.9 (a-a') Showing the accumulation mode operation of N-TFT and (b-b') displaying the same operation for P-TFT.

1.8 Techniques and Methods used TFT Film Deposition

In this section, several methods and techniques are mentioned which are used for the development of thin film upon substrate materials. In our work, PBTTT-C14 has played the role of organic semiconductors has it exhibits properties such as it can developed over different substrates even on PET substrate which is flexible in nature, low processing temperature, low production cost, good crystallinity and air stability, etc [58]. Along with this, PBTTT-C14 also demonstrate high sensing responses to gases as hydrogen sulfide, rending it for sensing applications [59]. With the help of **Figures 1.10-1.13** different technqiues and methods are shown for the development of thin film semiconductor devices.

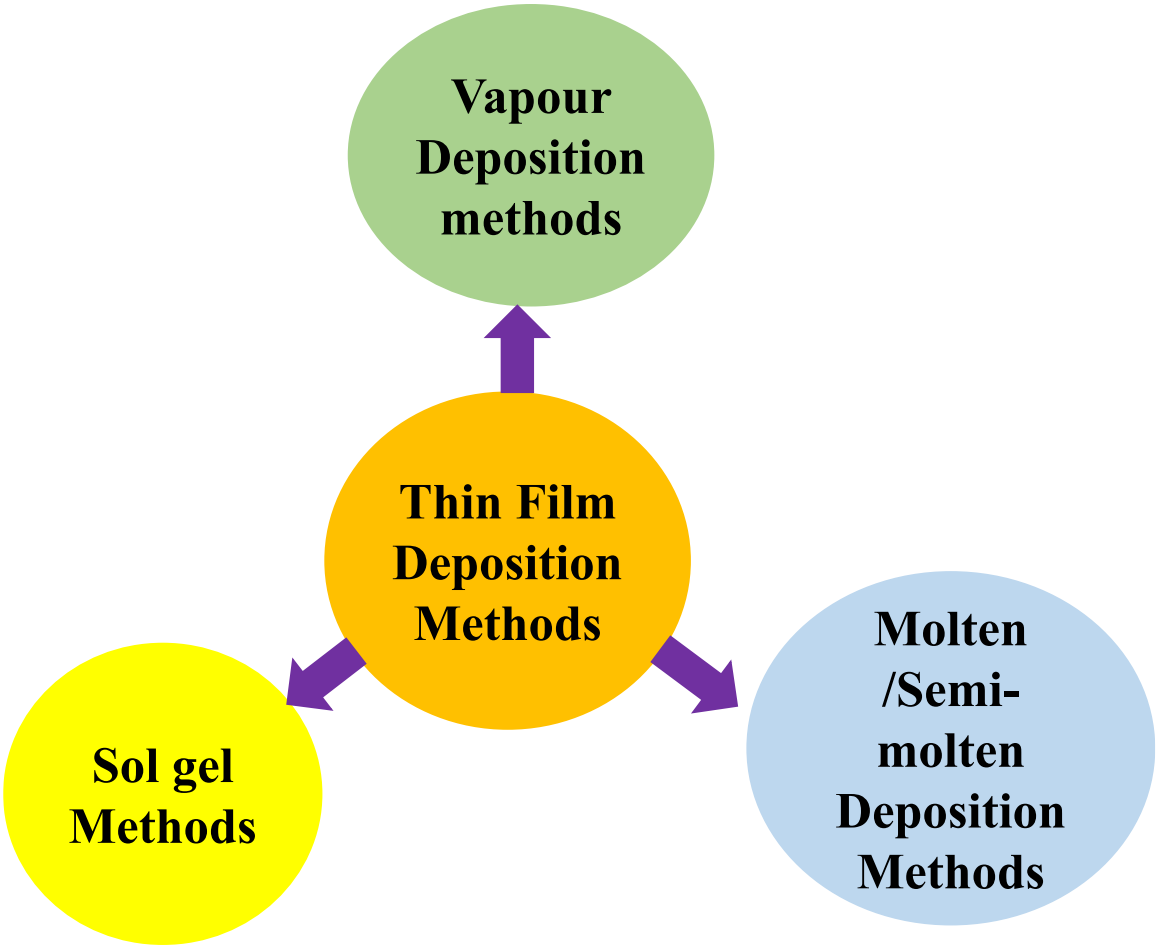


Figure 1.10 Classified Form of Thin Film Deposition Methods [60].

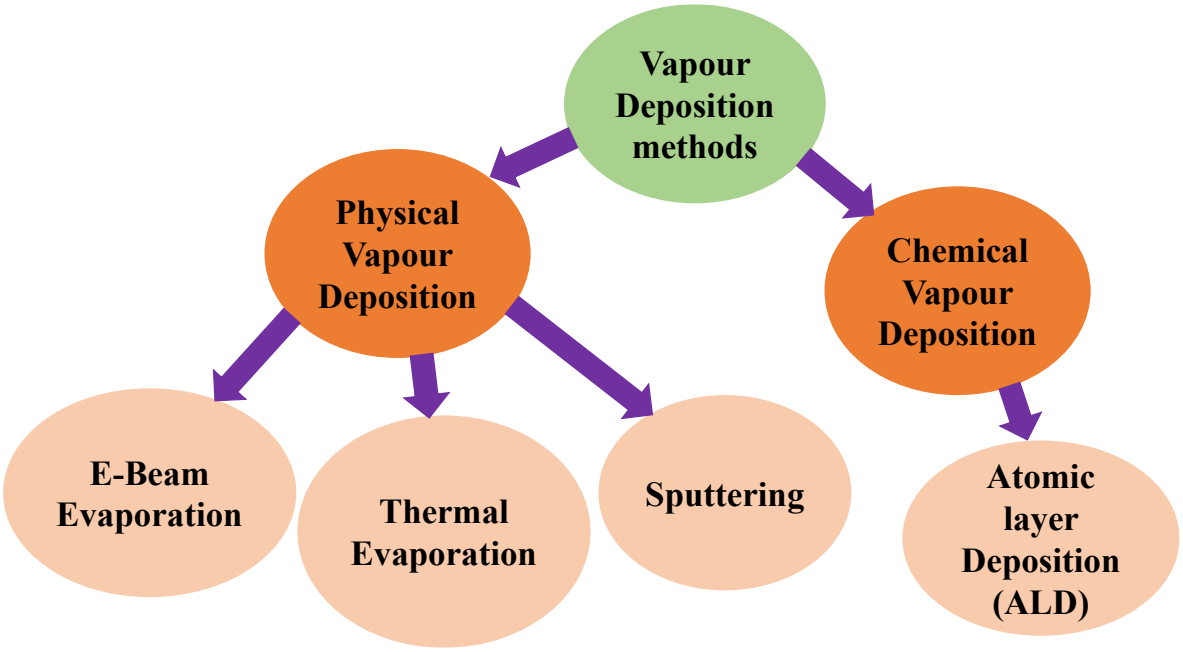


Figure 1.11 Classified Form of Vapour Deposition Methods [61], [62].

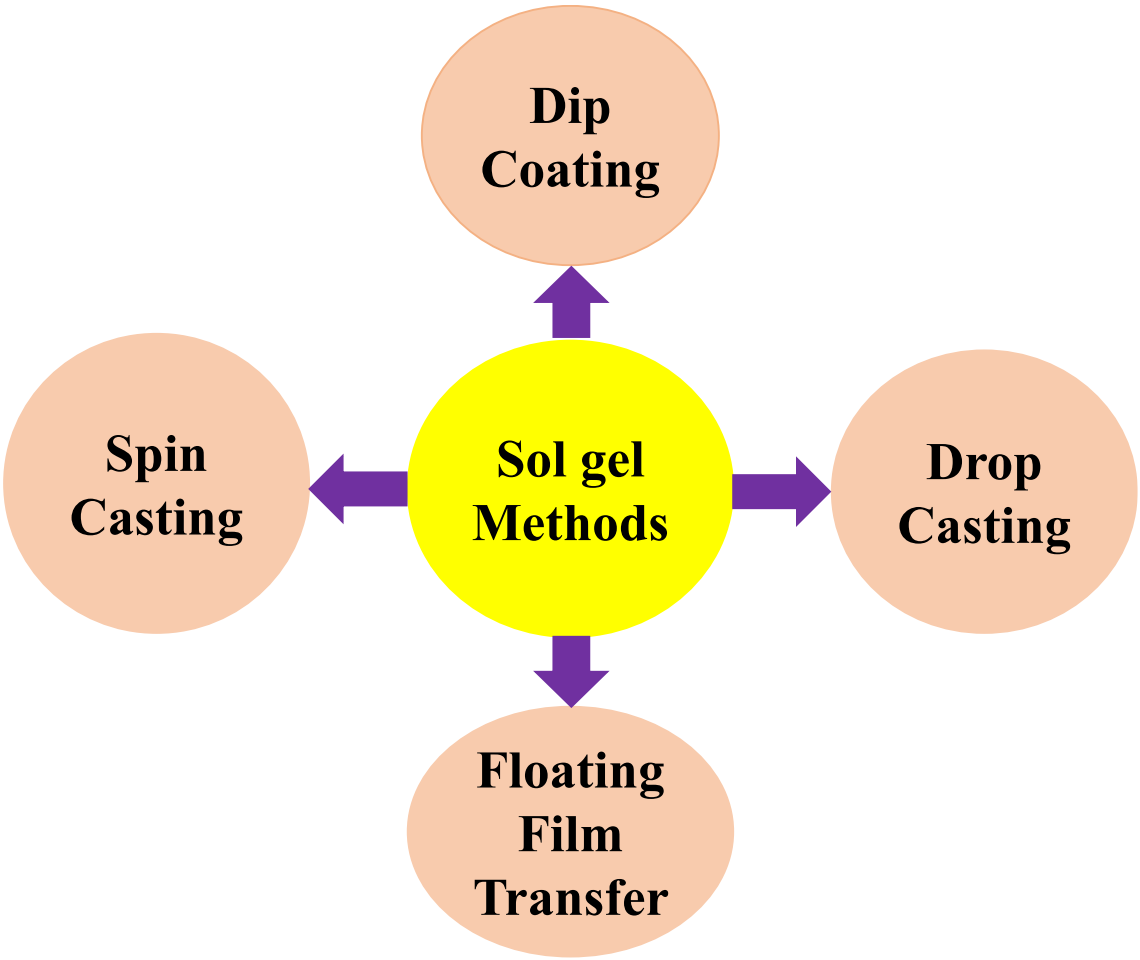


Figure 1.12 Classified Form of Sol gel Methods [63], [64].

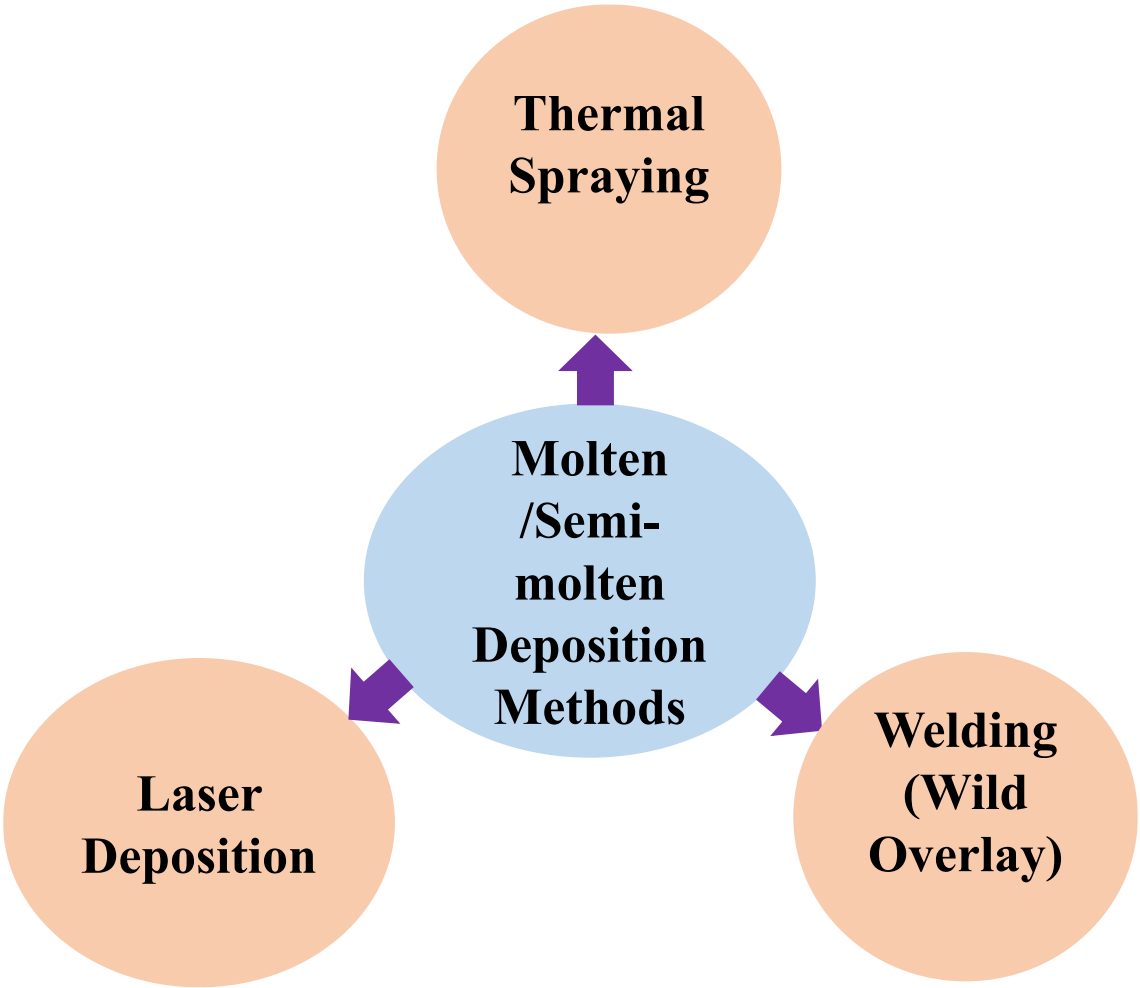


Figure 1.13 Classified Form of Molten/Semi Molten Deposition Methods [65]–[67].

In our work, for the development of active layer of TFT, we have opted FTM (Floating Film Transfer) methods for depositing film of semiconductor. This FTM methods exhibits many features as solution-processed in nature, cost-effective, negligible amount of solution-wastage, independent of instrumentation-setup. In the upcoming **Figure 1.14** the working from initial step to the development of film is shown there.

Floating Film Transfer Method

The FTM technique is highly preferred by many researchers as they possess features such as small fraction of wastage, simplified fabrication procedure and can be established upon various substrate materials [68]. Additionally, favors the self-assembled of polymer

molecules resulted helpful in obtaining organized ordered structure. Along with this, several factors such as alignment of polymer chain, film thickness across the substrate and crystalline properties are regulated and governed by this FTM technique. Using this technique thiophene polymer as PBTTT-C14 has been used for the development of semiconductor film over substrate. Several factors impact the formation of polymer crystal in film floating on liquid interface such as thermal gradient, relative viscosity, coefficient of spreading, solvent surface energy, etc. Hence, in our work we have opted the concept of surface energy for the establishment of PBTTT-C14 polymer film on the liquid medium of ethylene glycol and glycerol mixed in the proportion of 1:1 which is shown in **Figure 1.14 (a)**. A flow chart is showed in the figure which states the working mechanisms of FTM Method. Based on Marangoni flow principle, solvent exhibiting low surface energy naturally spread in comparison to the solvent having higher surface energy. This flow principle has been applied here for the establishment of self-assembly and directional growth of PBTTT polymer upon liquid medium of Ethelene glycol and glycerol having ratio of 1:1. Small magnitude of solvent surface energy can be caused by surface pressure gradient, which be produced by the introduction of solvent having low surface energy (PBTTT dissolved in chloroform solution in this work) with the help of which this PBTTT film spreading would take place shown in **Figure 1.14. (b).**

Two forces would come in action and their behavior decide the formation of film named as 1. Driving force 2. Viscous force. When driving force (F_D) dominates the viscous force (F_V) smooth spreading would take place and thin film is obtained ($F_D > F_V$). On the other hand, when viscous force (F_V) leads the driving force (F_D) coagulation would happen which is not suitable for development of film. These two conditions are shown in **Figure 1.14 (c)**. In **Figure 1.14 (d)** entire film developed over gate dielectric is displayed.

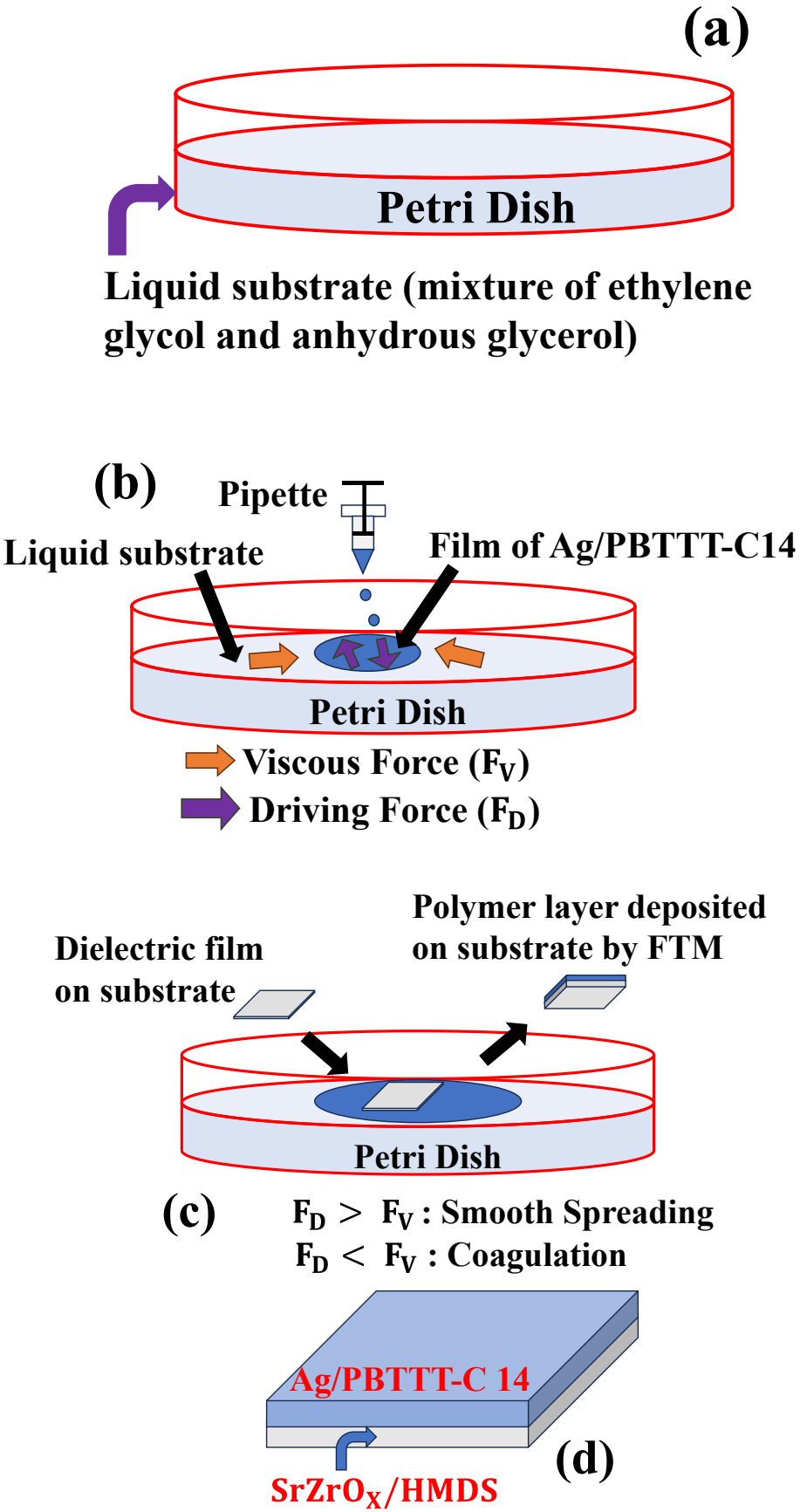


Figure 1.14 (a-d) Showing the step involved in FTM techniques for film deposition.

1.9 Compact Modeling of TFT Devices and Previous History of Compact Modeling

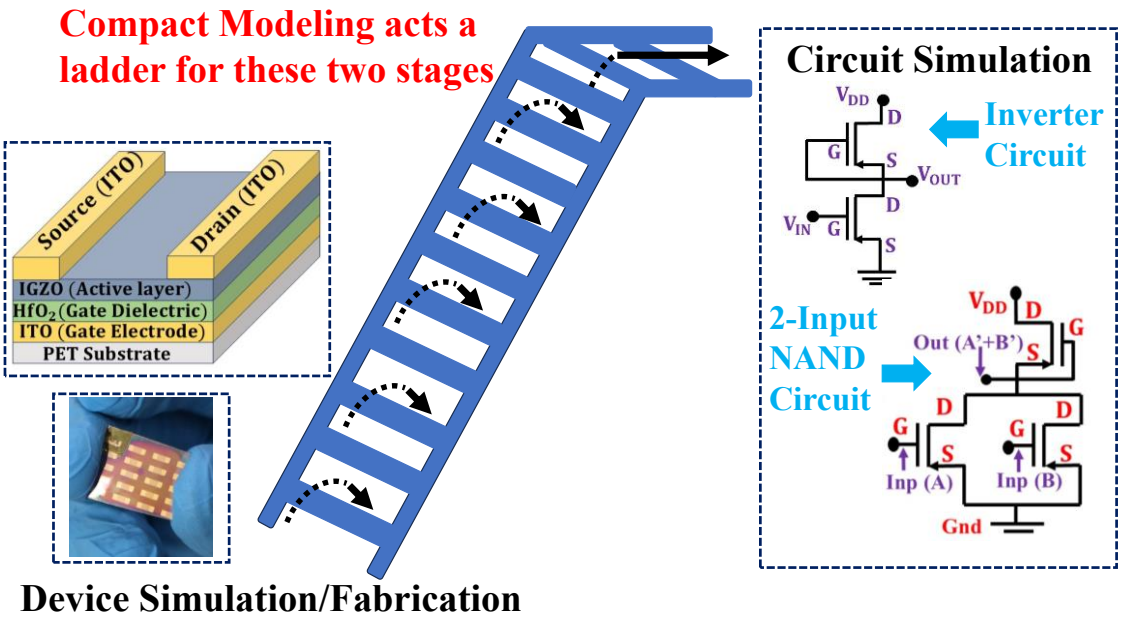


Figure 1.15 Showing an overview and important role of compact modeling for realization of circuits.

The ultimate goal of any fabricated/simulated TFT device is that it would be further used for realizing analog/ digital circuits and integrated circuit (IC) designing. This gap of device fabrication/simulation and circuit implementation is fulfilled by compact modeling by acting as bridge between these two stages [69]–[71]. Compact model exhibits all the device features, physical properties and device terminals, mathematical representation of TFT which would used in for circuit implementation. This compact model is an essential part for designing IC parts [72], [73]. For the proper function and realization of analog/ digital circuits compact model should posses these features as follows [72]–[74]:

- Behaviour is presented in consistency manner.

- Symmetrical nature to exhibit TFT structure.
- Less complexity and easily approachable, derivable.
- Compact Model is admissible to other types of TFT's also.
- Characterization of the parameters can perform in easy way.
- All the relations existed can be easily justified.

For designing circuit different kinds of softwares were used as Cadence, SPICE, etc. The model reside in this software acts as fundamental unit of the device for circuit designing [69]–[71]. In 1983, Kacprzak and the team has done compact modeling for the first time in which GaAs FET was DC modeled for the estimation of large signal in computers [75]. After this innovation many research worked in this domain of compact modeling of device and in the upcoming year 1986, 1-D Poisson equation based compact model for the poly-silicon device operated in accumulation mode was reported by Ahmed and team [76]. For poly-Si TFTs, A unified model has established by Benjamín Iñiguez and team in 1999, the model is based on effective medium approximation for long channel and short channel of poly-Si TFT devices [77]. In the same year, another model was proposed by Mark Jacunski and the team, in which semi empirical analytical model is developed for compact modeling of poly silicon TFT. This model explains 4 regions of operations as leakage, subthreshold, above threshold and kink [78].

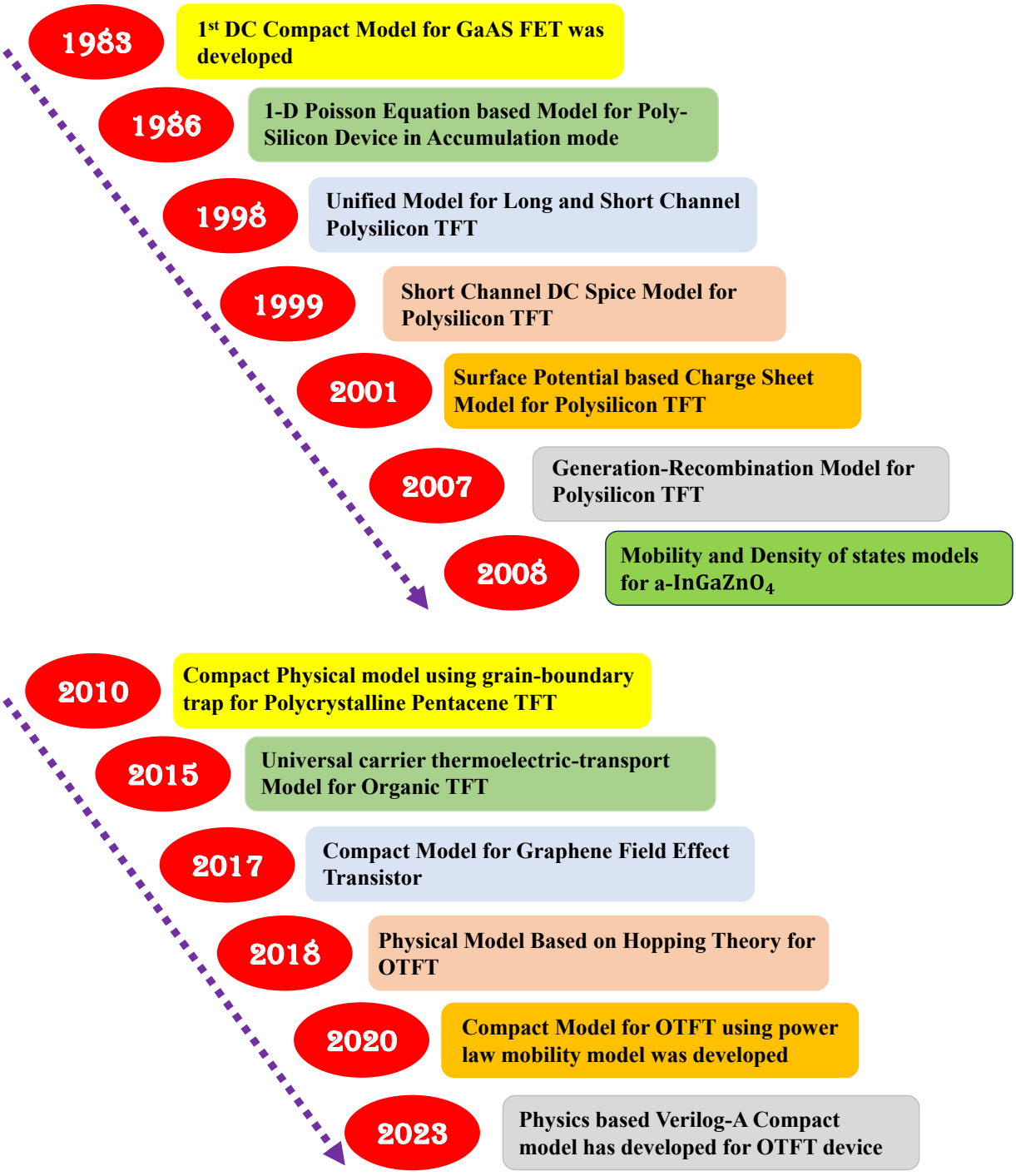


Figure 1.16 Journey and Innovation of Compact modeling for organic and inorganic TFTs.

In 2000, M.J. Siddiqui and the team developed DC charge sheet model in which large numbers of equations are used for compact modeling of Poly silicon TFTs [79]. In 2007,

Weijing Wu and the team developed generation-recombination model which includes both poole Frenkel- effect and phonon tunnelling for poly silicon TFT [80]. In the same year, after so many models developed for poly-silicon TFT, different models were founded by researchers for several devices as Chaitanya Sathe and Santanu Mahapatra has proposed model, in which (Mahapatra-Ionescu-Banerjee) MIB model has been used for compact modeling of Single Electron Transistor based on Static Noise Margin. Noise Margin is estimated using in terms of capacitances and impact of temperature on Noise Margin has been noticed [81]. In 2008, Hsing-Hung Hsieh and the team has done the compact modeling for a-IGZO TFT. In this constant mobility model and subgap density of states models are used for the compact modeling of a-IGZO based TFT [82]. In 2009, generic analytical modeling that is charge drift model is used for compact modeling of all regions of OTFT, was reported by Ognian Marinov and the team [74]. Ling Li and the team reported compact modeling for OTFT in 2010, Pentacene TFT in which modeling was based on barrier height model with Gaussian energy distribution of traps at grain boundaries for both linear and saturation regions were developed [83] . Along with this, impact of temperature was also observed. In 2011, For the realization of complex circuitry as shift register, W. S. Zhao and the team has established compact model based on magnetic tunnel junction (MTJ) domain wall was proposed for the implementation of shift register [84]. In 2014, J. A. J. Tejada and the group of researchers was reported compact modeling of OTFT which has done including contact effects for the

determination of parameters as mobility (μ) and threshold voltage (V_{TH}) [85]. In 2015, Nianduan Lu and group of researchers has developed an analytical model named as Universal carrier thermoelectric-transport model based on percolation theory in organic semiconductors that explain the seebeck feature of organic semiconductor for both disorder free and general disorder transportation [86]. In the same year, A. Valletta and the team developed DC compact model for OTFT device is based on channel length approximation, contact effect at semiconductor and metal contacts. Using this model Inverter circuit and ring oscillator has been simulated on Spice Platform [87]. In 2015, M. Ghittorelli and group of researchers has developed physics-based analytical model for the charge transportation across the channel and the injection of charge carrier at the source for IGZO TFT device [88]. In 2019 and 2020, Using paper Unified Model parameter Extraction Method (UMEM) compact model for IGZO TFT devices has developed by W. E. Muhea and team. These models are based on theory of density of states, tail states and deep density of states, low frequency [89], [90]. In the same year 2020, using the same UMEM approach Harold Cortes-Ordóñez and the team has developed power law mobility model for compact modeling of OTFT and parameter extraction is done such as threshold voltage (V_{TH}), mobility (μ) , subthreshold slope (SS) [91]. In addition to this, Sungyeop Jung and group of researchers reported a review paper which compares the previously reported papers related to compact modeling of OTFT device [92]. In 2023, Alexander Kloes and the team proposed Physics based Verilog A

Compact Modeling for OTFT has been done in this paper including charge-based capacitance model for the regions of short-channel as overlap and fringing regions. Along with this, modeling of drain current, low-noise frequency and noise-quasistatic effect, short and long channel is done [93].

TCAD (Technology computer-aided design) based Compact Modeling Using Silvaco-Techmodeler tool

In this work, compact modeling of both a-IGZO device and OTFT device has been performed using Silvaco-Techmodeler tool.

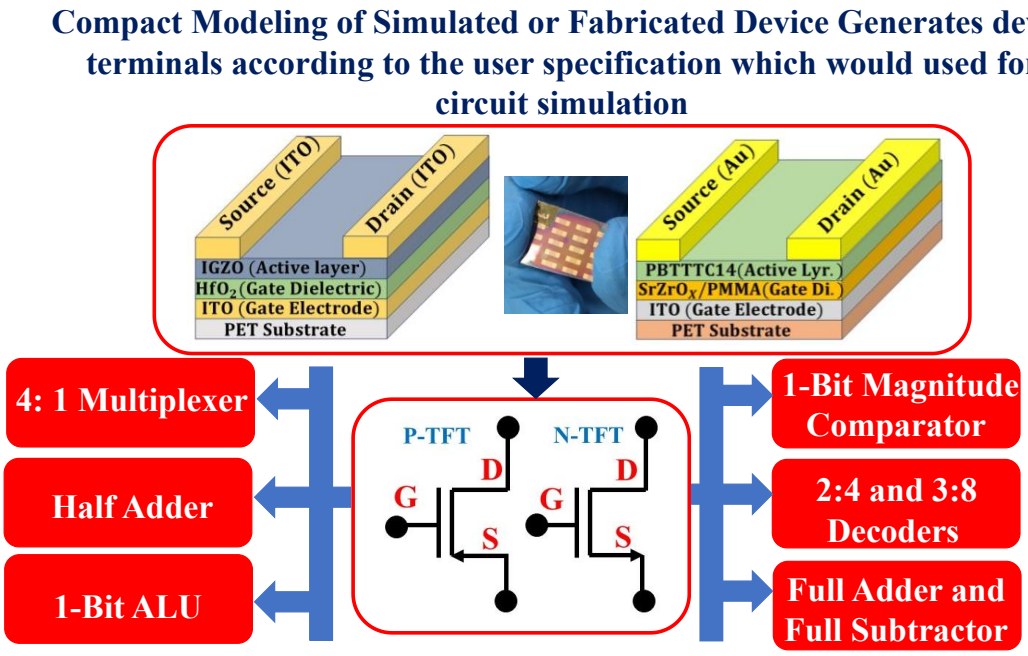


Figure 1.17 Showing different types of combination circuits implemented using this Compact modeling technique [94]–[100].

This compact modeling based on behavior modeling technique in which device specifications are provided by the user and the complier is designed in such as way that

it has a module which solves all the complex mathematical calculations which user has to solved by itself in previous models [101]. These models are terms as black-box models. Additionally, this compact modeling approach is free from all types of typical mathematical complexity and others constraints as material, contact effects, etc. Along with this compact modeling of this device, a device prototype has also developed by the complier which carries all the device specifications and properties which is further exported at Silvaco-Gateway tool for the realization of complex analog and digital circuits.

Stages involved in behavior modeling flow are explained as follows:

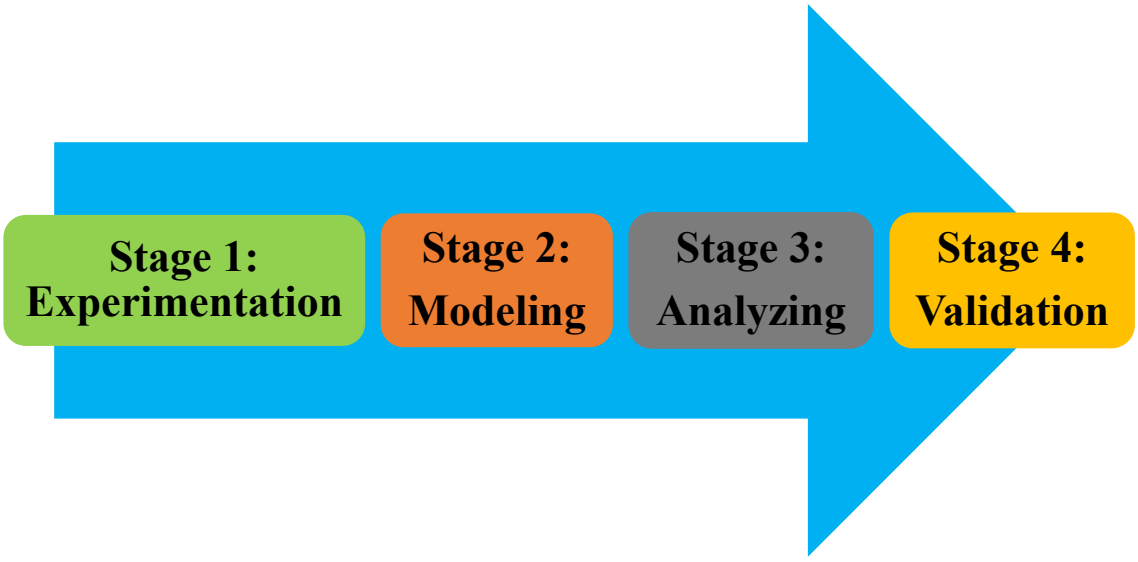


Figure 1.18 Showing the flow of TCAD device modeling process in different stages.

1. **Experimentation:** In this step, the results of simulations and experiments are provided to the tool. In **Figure 1.19.** The obtained device characteristics are given to the tool.

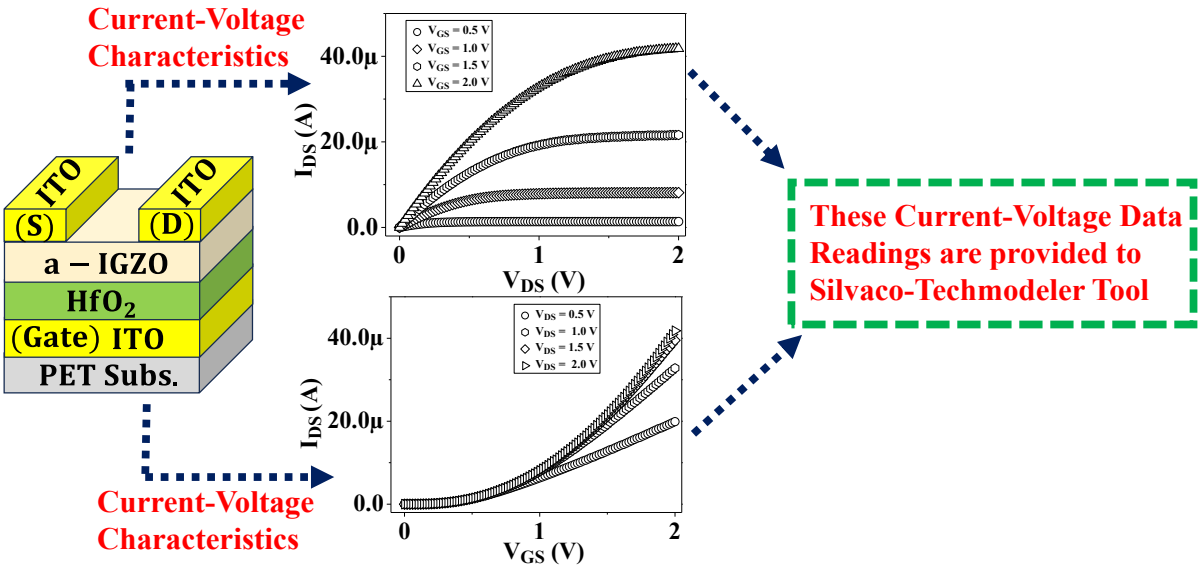
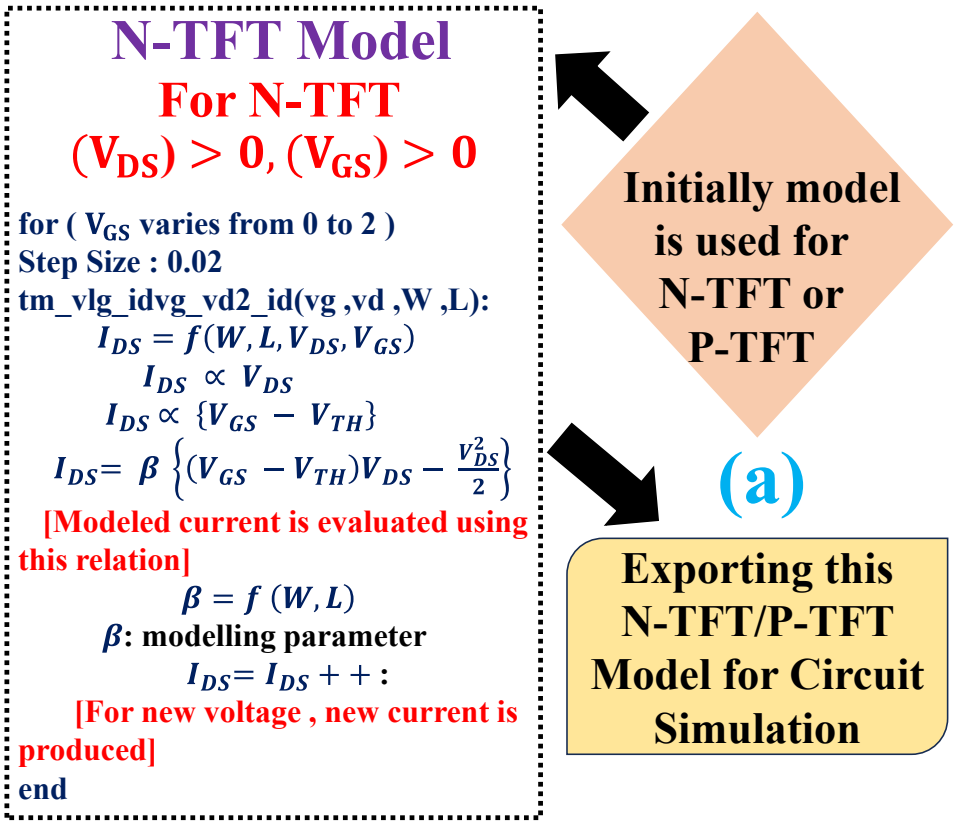
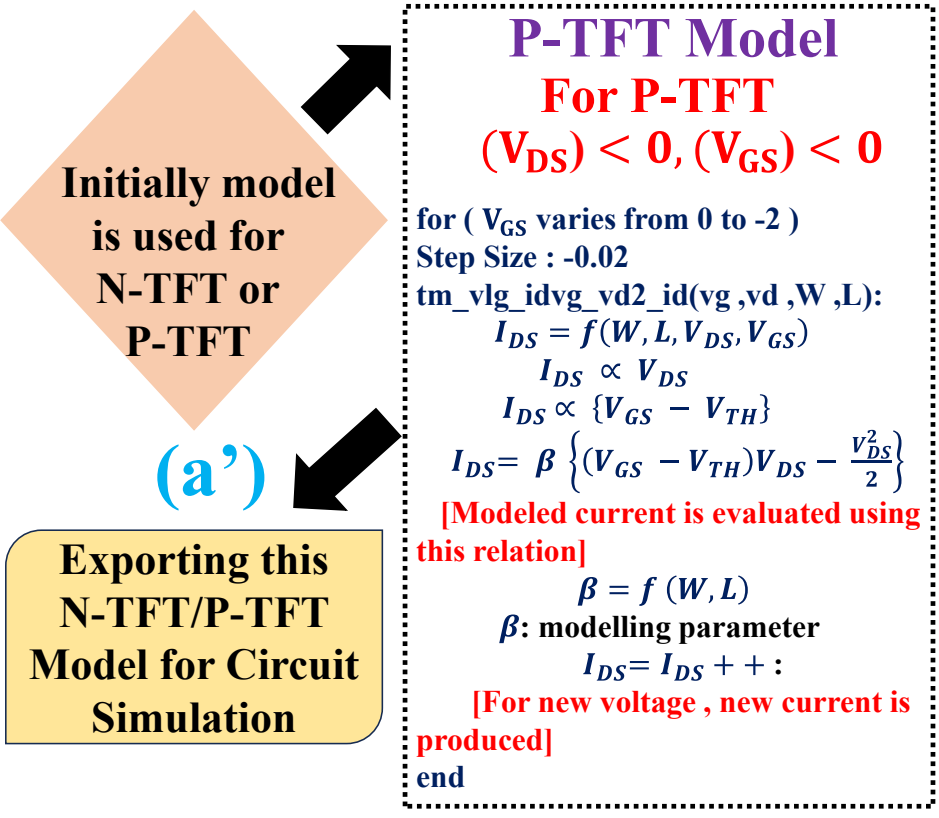


Figure 1.19 Step 1 in which data points of current-voltage are supplied to Silvaco-Techmodeler Tool.

2. Modeling: In this step, according to the opted model (N-TFT or P-TFT), corresponding equations are used for the simulation of modeling data, which is expressed in **Figure 1.20.**

In **Figure 1.20 (a),** the complier first checks which type of model is to be opted either N-TFT or P-TFT that depends upon the applied voltage for $V_{DS} > 0$ and $V_{GS} > 0$ the model would be N-TFT otherwise for $V_{DS} < 0$ and $V_{GS} < 0$ it would be proceeded for P-TFT. Similarly **Figure 1.20 (b)** showing the format in which the user provided the data points and device specifications to this Silvaco-Techmodeler tool as width (W), length (L), gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). In **Figure 1.20 (c)**, with the help of transfer characteristics which is provided by the user, the complier has taken the square root of the drain current points in order to estimate the threshold voltage (V_{TH}). Now all the required parameters are now known, using modeling equation shows as **Figure 1.20 (a)**, model current is estimated according to different-different voltage points.


N-TFT Model
For N-TFT
$(V_{DS}) > 0, (V_{GS}) > 0$
for (V_{GS} varies from 0 to 2)
Step Size : 0.02
tm_vlg_idvg_vd2_id(vg ,vd ,W ,L):
$I_{DS} = f(W, L, V_{DS}, V_{GS})$
$I_{DS} \propto V_{DS}$
$I_{DS} \propto \{V_{GS} - V_{TH}\}$
$I_{DS} = \beta \left\{(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right\}$
[Modeled current is evaluated using this relation]
$\beta = f(W, L)$
β: modelling parameter
$I_{DS} = I_{DS} + +$:
[For new voltage , new current is produced]
end
Initially model is used for N-TFT or P-TFT
(a)
Exporting this N-TFT/P-TFT Model for Circuit Simulation


P-TFT Model
For P-TFT
$(V_{DS}) < 0, (V_{GS}) < 0$
for (V_{GS} varies from 0 to -2)
Step Size : -0.02
tm_vlg_idvg_vd2_id(vg ,vd ,W ,L):
$I_{DS} = f(W, L, V_{DS}, V_{GS})$
$I_{DS} \propto V_{DS}$
$I_{DS} \propto \{V_{GS} - V_{TH}\}$
$I_{DS} = \beta \left\{(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right\}$
[Modeled current is evaluated using this relation]
$\beta = f(W, L)$
β: modelling parameter
$I_{DS} = I_{DS} + +$:
[For new voltage , new current is produced]
end
Initially model is used for N-TFT or P-TFT
(a')
Exporting this N-TFT/P-TFT Model for Circuit Simulation

Initially, all the device specifications such as width (W), length (L), V_{DS}, V_{GS}, drain current (I_{DS}) of transfer characteristics obtained using simulation / fabrication are provided to Silvaco-Techmodeler tool.

(b)

```
% File../idvg_igzovd2.dat
% Column names: VG ID VD W L
% Name: idvg_igzovd2
% Rows: 101
% Columns: 5
0.00  4.43E-10  2  180E-6  30E-6
0.02  8.89E-10  2  180E-6  30E-6
0.04  1.79E-09  2  180E-6  30E-6
0.06  3.45E-09  2  180E-6  30E-6
.....  .........  .....  .....  .......
.....  .........  .....  .....  .......
```

This algorithm plots the transfer curve (I_{DS} - V_{GS}) from the data points provided by user and through this transfer curve ($I_{DS}^{0.5}$ - V_{DS}) is plotted for the estimation of the threshold voltage (V_{TH}).

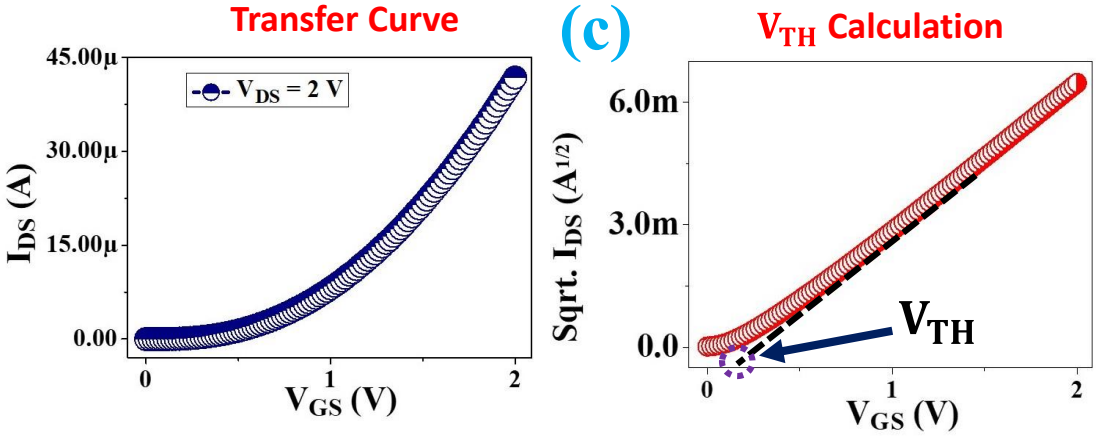
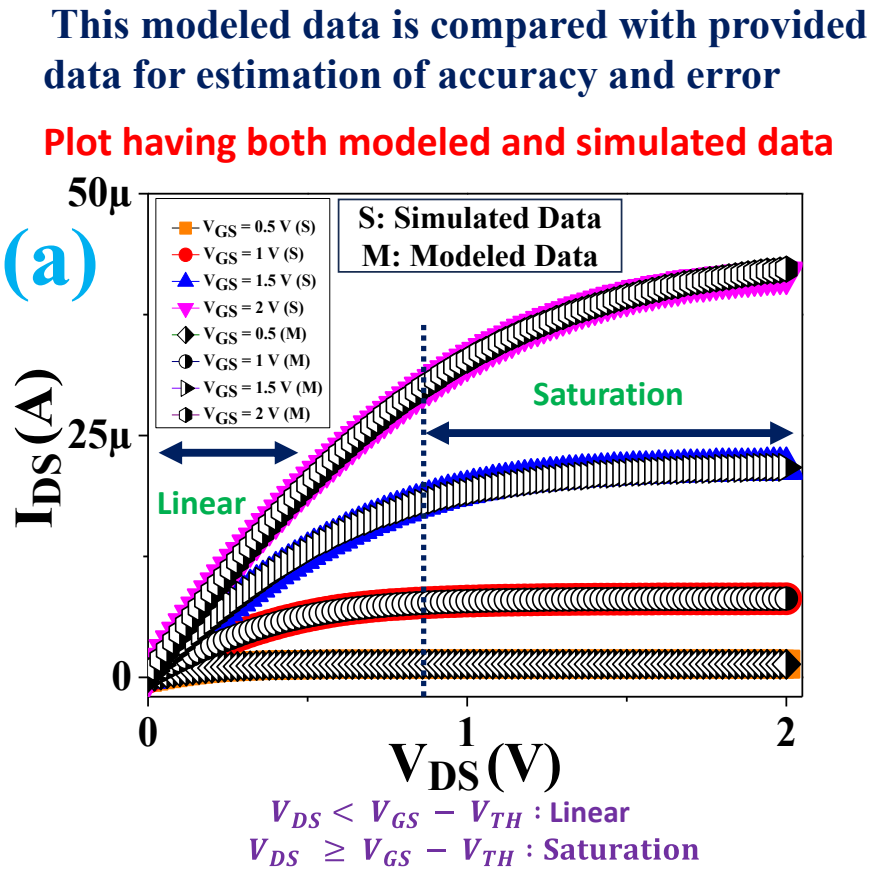


Figure 1.20 (a-c) Step 2 in which different stages exist for the execution of modeling section.

3. **Analysis:** In this section, analysis is performed by estimating the percentage of error versus the supplied data points. Furthermore, errors are estimated between

modeled and experimental or simulated data. Exported model can be used for further analysis. In **Figure 1.21.** The details associated with analysis stage is shown.



In **Figure 1.21 (a)** Showing the plots of both simulated and modeled data, all the curves of both simulated and modeled data completely superimpose on each other which states that very small fraction of error (less than 1%) is between them and exhibits high accuracy. **Figure 1.21 (b)** Showing the exported N-TFT model which carries all the devices specification shown in Stage-2 that is modeling and in **Figure 1.21 (c)** Inverter circuit is simulated using this exported N-TFT model and transient Analysis has also performed which verifies inverting behaviour for both inputs '0' and '1'.

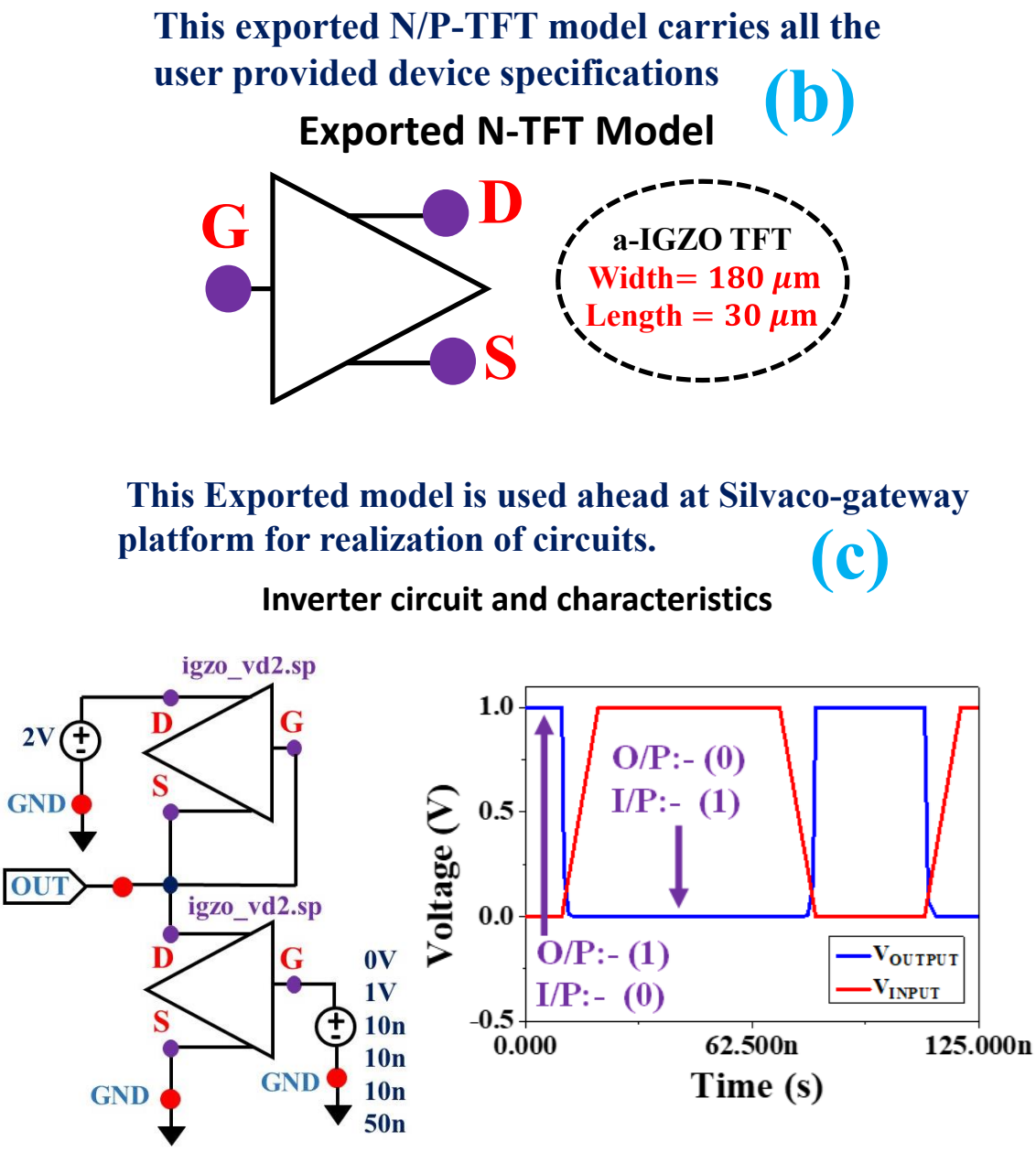


Figure 1.21 (a-c) Step 3 in which analysis section is done where device prototype has been exported for circuit simulation.

4. **Validation:** Both modeled and experimental/simulated data are verified by the superimposition of both curves on each other. In **Figure 1.22.** Curves of both simulated and modeled data is shown.

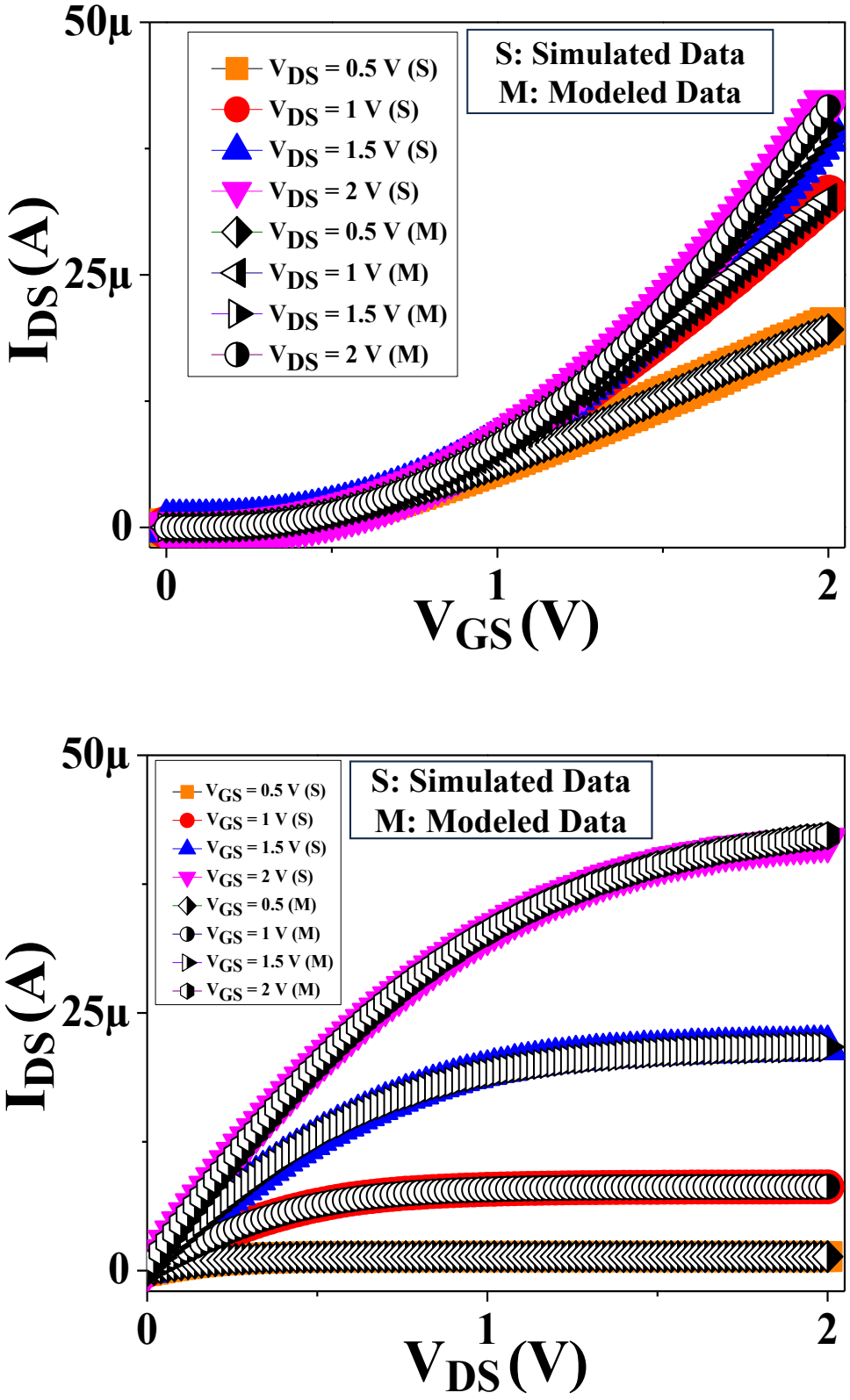


Figure 1.22 Step 4 in which both the cures are validated, the superimposition of these curves confirm small error is exist between them.

After the validation stage, the performance report is exported, in which all the data points of the experimental, simulated, and modeled curves exist. Along with this, smart-spice files (.sp) and verilog files (.va) can also be exported that contain all the user specifications, i.e., in this case, operating voltage, width, length of device, etc. These (.sp) and (.va) files are further used at the Silvaco-Gateway tool for the realization of circuits.

1.10 TFT Applications

For developing a TFT device many configurations and structures are possible which resulted very helpful in realizing several applications [5], [22], [23], [25], [102]. Along with this, substrates as PET, PEN are used for utilizing in for the applications of flexible electronics [103]–[105]. Additionally, large variety in available for semiconductor materials and insulator materials. All these choices options related to materials; substrates and cost-effective device production have gathered high attention of researchers towards TFT. All these advantages mentioned above led to TFT device for essential application as shown in these articles mentioned above.

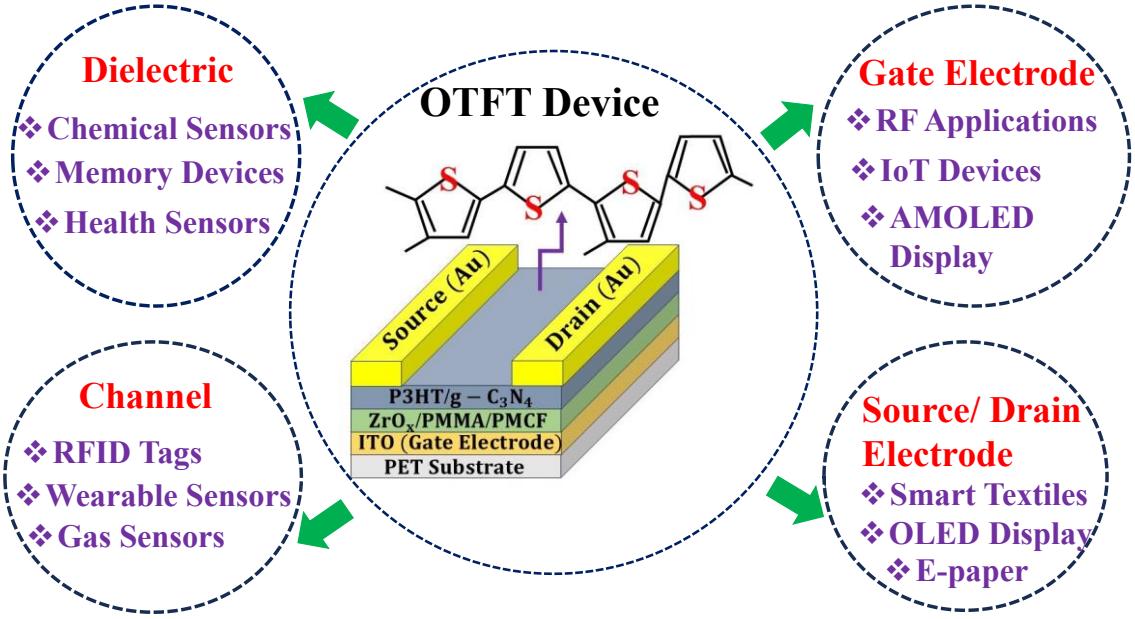


Figure 1.23 Stating various application of TFT structures.

The tailoring in materials properties of TFT led to the development of detectors, sensors, etc. The governance of the charge-carrier of TFT facilitates many researchers in developing several sensors as optical, magnetic etc. Similarly, by the utilization of organic semiconductors and substrates as PET, PET explored TFT in the field of Flexible Electronics. The production of TFT is cost-effective in nature helps many users to develop memory circuits, IC designing, display circuits, etc [106]–[108].

1.11 Thesis Outline

The ultimate goal of this thesis is to explain to fabrication and simulation of TFT devices with the help of organic and inorganic materials that are operated at low-voltage and for further utilization in sensing and electronics applications. Nowadays, the rise of high demand of light weight device and flexible nature is increased therefore, for the easy of understanding different techniques, methods involved for the fabrication of TFT devices are explained in a detailed manner.

This thesis is divided into seven chapters which carries all the research analysis performed during the PhD phase. It starts with the history, working principles of device and associated key-mechanisms, modern technology, device fabrication, device simulation, compact modeling of simulated / fabricated devices and its applications.

Chapter 1: In this chapter the background associated with device, its working, basic-mechanisms have elaborated. The key-points are as follows:

- *Background related to Thin Film Transistors*
- *Device working and basic of Thin Film Transistors.*
- *Advantages and Disadvantages of Organic and Inorganic Semiconductors.*
- *Techniques and materials involved*

- *Compact Modeling and Its Importance*
- *TFT Applications.*

Chapter 2: In this chapter, the fabrication of Organic Thin Film Transistors developed upon silicon substrate is explained. These fabricated OTFT are operated at low-voltage and utilized for gas sensing application. All the steps in required for film, electrode deposition is expressed in an elaborative manner. The background associated with device, its working, basic-mechanisms have elaborated. The key-points are as follows:

- *Ag doped PBTTT-C14 based OTFT has been fabricated on silicon, operated at 1.5 V which is used for the sensing of H_2S gas.*
- *$SrZrO_X$ is used as gate dielectric for Ag/PBTTT-C14 based OTFT.*
- *Characteristics related to device; film are also explained.*
- *FTM Methods used for development of these devices which is cost-effective and solution-processable in nature.*

Chapter 3: In this chapter, the fabrication of flexible Organic Thin Film Transistor is shown which exhibits flexibility and bending features. This flexible fabricated OTFT are operated at low-voltage ~ 1.0 V and utilized for electronics applications. All the steps in required for film, electrode deposition is expressed in an elaborative manner. The key-points are as follows:

- *PBTTT-C14 based OTFT operated at 1.0 V has been fabricated on PET Substrate for flexible device.*
- *$SrZrO_X$ and PMMA is used as gate dielectric for this PBTTT- C14 based OTFT.*
- *Characteristics related to device; film are also explained.*
- *FTM Methods used for development of these devices which is cost--*

-effective and solution-processable in nature.

Chapter 4: In this chapter, fully-transparent flexible low voltage TFT has been simulated using Silvaco-Atlas tool. All the materials used for the simulated of fully transparent device has been explained, furthermore the device has been compact modeled using Silvaco-Techmodeler tool which is used ahead for electronics applications. The key-points are as follows:

- *a-IGZO based TFT has been simulated in which HfO_2 and ITO acted as dielectric and electrodes and substrate is PET.*
- *Operating voltage of the device is 2 V*
- *Defects states associated with a-IGZO are also explained*
- *An Introduction to Compact modeling.*
- *Stages of compact modeling using Silvaco-Techmodeler tool*
- *Error estimation between simulated/fabricated data and modeled data.*
- *Importation of model for Simulation of Full Adder and Full Subtractor circuit is explained*
- *The Truth Table of these combinational circuits are also verified*.

Chapter 5: In this chapter, Silvaco-Techmodeler and Silvaco-Gateway tools are explained, which are platforms in which compact models of simulated/fabricated devices have been used for the implementation of logic circuits.Characteristics of circuits can also be observed such as transient and DC characteristics for the estimation of noise margin analysis, gain, delay estimation, truth table verification. The key-points are as follows:

- *Introduction to Silvaco-Techmodeler and Silvaco-gateway tools and importing of compact modeled file of simulated/fabricated device at*

this tool.

- *Familiarization with the pre-existed library which carries components as supply voltage, wires, etc.*
- *Implementation of circuits as Half adder, Half Subtractor, Inverter, 4:1 Multiplexer, 2:4 Decoder, 3:8 Decoder, Logic gate families, 1- Bit Magnitude Comparator, etc.*
- *Verification of Truth table of respective Combinational Circuits.*
- *Voltage Transfer and Transient Characteristics has also performed to calculate propagation delay, inverter gain, etc.*

Chapter 6: In this chapter, Stability analysis is performed in which factors impact on the device stability as thickness of active layer, thickness of gate-dielectric, fixed charge density of dielectric is observed using Silvaco-Altas tool. The key-points are as follows:

- *Simulation of a-IGZO based TFT operated at 1.5 V using Silvaco-Atlas tool.*
- *Impact of Thickness of active layer and dielectric on the Change in Threshold Voltage* ΔV_{TH} *for stress time of 0,600, 1200,1800, 3600,5400 and 7200 seconds.*
- *Impact of fixed charge density of dielectric on the Change in Threshold Voltage* ΔV_{TH} *for stress time of 0,600, 1200,1800, 3600,5400 and 7200 seconds.*

Chapter 7: This chapter, summarizes the research work of all the chapters explained above. Additionally, in this chapter the additional scope of this field is shown for the additional investigation and analysis.

Chapter 2

Fabrication of Ag-Doped PBTTT-C14 Low-Voltage OTFT for H_2S Gas Detection

2.1 Introduction

Nowdays, it has been noticed that Natural Gases, Petroleum Industries, and Kraft Paper mills become victims of explosives and accidents because of forming Hydrogen Sulfide (H_2S) which exhibits dangerous properties such as toxicity and flammability, leading to healthcare issues for the flora and fauna. The low concentration of H_2S results in health issues such as eye infections, throat injuries, respiratory problems, weak memory, and other lot no of issues and consequences to the human beings. A higher concentration of H_2S gas for some minutes such as 1000 ppm for 10 minutes (parts per million) can leads to sudden death [109]–[111]. Even H_2S-based sensors still exist with us but have various drawbacks such as high cost (100-1000), high power consumption, and some are restricted to particular high temperature ranges [111]–[113]. As per the benchmark specified by the American Conference of Government Industrial Hygienists (AGIH) from the safety perspective bearing capacity of humans for H_2S gas is 10 ppm. H_2S gas at workplace is risky and damaging, according to the Occupational Safety and Health Administration and the Bureau of Labor Statistics [114]. Hence, from the safety perspective in the fields of environment and industries, it is important for the detection of H_2S gas [115], [116]. Nanowire Field Effect Transistors based on inorganic semiconductor material are also developed as gas sensors [117], [118]. For the detection of low concentrations of gases at room temperature, OTFTs (Organic Thin Film Transistors) have gained much more attention as it offers various excellent properties such as flexibility, high selectivity, high sensitivity observed at low cost fabrication

process [119]. In the past several years organic polymer TFT devices have been utilized in various sensing applications [120]. In today's era, SiO_2 based OTFT electronic gas sensors are typically power-hungry [121], hence it become essentials that fabricated gas sensors are operated at low voltage (preferably 1-2 V). Along with that, the surface roughness of dielectric film and channel had a crucial impact on OTFT's electrical performance and also in sensing operations [122]. In most OTFT devices, SiO_2 is commonly used oxide film as a gate oxide layer because it offers smooth surface roughness, good oxide semiconductor interface, etc. However, an oxide capacitance associated to SiO_2 is quite low due to a small dielectric constant (k~3.9), which makes OTFT devices power-hungry [121], [123]. In order to reduce the operating voltage of OTFT with SiO_2 as a gate oxide, the thickness of oxide should be reduced, which can increase oxide capacitance. But on the other side the reduced oxide thickness can causes tunneling gate leakage current and deteriorates the device performance. Hence, to suppress the tunneling gate leakage current and fulfill the requirement of low operating voltage of OTFT, a high-k dielectric with a high dielectric constant (k>10) is preferred as a gate oxide with a certain thickness over other conventional dielectric such as SiO_2 [124], [125]. Therefore, choosing a dielectric material has become essentially important, especially for low-power devices and it can be chosen based on the following criteria [126], [127] :

1. The dielectric material should have a k value between 10 to 30 and also free from the short channel effects.
2. Dielectric materials also offers a band gap of at least 5 eV.
3. Dielectric possesses a low interface trap density ($< 10^{11}$ cm^{-1} eV^{-1}).
4. Oxide consisting surface energy change should be in range of (ΔG) = (0 to -

50KJ/mol) exhibits a weak tendency of water absorption and is comparatively stable and suitable for OTFT devices with excellent performance.

In this work, an organic thin film transistor (OTFT) fabricated via solution processing methods. It is operated at low voltage and has been utilized for H_2S gas sensing at room temperature (~25 ºC). As ZrO_2 has a band-gap of 5.8 eV., (ΔG = -47 KJ/mol) and a dielectric constant value of ~25 [123], [126], [127]. OTFT has been used for the application of gas sensing for sensing various gases such as ammonia (NH_3), sulfur dioxide (SO_2), and $NO_{2.,}$ hydrogen sulfide (H_2S). This becomes possible due to the polymer-based active layer helping in the detection of gases. For detection of the toxic gas, metal oxide (MO_X) based material can be used especially for H_2S sensing but with some restrictions such as strong dependency over relative humidity (RH) and usually operated at high temperature (> 100 ℃). Therefore, conductive polymers are used as a replacement for it [114]. In this work, top contact bottom gate (TCBG) structured silver nanoparticles-doped poly (2,5- bis(3-tetradecylthiophen-2yl) thieno (3,2- b) thiophene) (PBTTT-C14) based OTFT operated at low voltage has been fabricated and utilized for H_2S gas sensing application at room temperature operation (~25 ºC) [128]. The novelty of the proposed work is fabricating a low voltage cost efficient, high performing OTFT based H_2S sensor without any complex or costly fabrication setups.

2.2 Chemical Required and Materials Synthesis

PBTTT-C14(Poly[2,5-bis(3-tetradecylthiophen-2-yl) thieno[3,2-b] thiophene]) (MW > 50k), strontium chloride and zirconium acetylacetonate were procured from Sigma Aldrich pvt. ltd. and used in OTFT fabrication without any further purification. The remaining necessary chemicals, including HMDS (Hexamethyldisilazane), cleaning agents, ethylene glycol ($C_2H_6O_2$), glycerol anhydrous 87% GR ($C_3H_8O_3$), and chloroform

($CHCl_3$), were purchased from Merck India Pvt. Ltd. The following synthesis steps are involved for OTFT fabrication including the synthesis of high-k dielectric and channel.

1): For the synthesis of high-k dielectric, separately, 300 mM of strontium chloride and 150 mM of zirconium acetylacetonate (Zr $(Acac)_4$) were dissolved in 2 methoxy ethanol in transparent vial tubes for the dielectric solution. For thorough mixing, the solution was continuously stirred at 1000 rpm for 6 hours at room temperature (RT-25 ^{o}C). After that, the prepared solution was mixed in separate vial tubes at a certain ratio of 1:6 and further kept on stirring at 1000 rpm for 6 hours for uniform homogenous mixing. The ratio of the solution has been optimized for enhanced surface roughness and dielectric constant of the film.

2): For the active layer 10 mg/ml of PBTTT-C14 and 1 mg/ml $AgNO_3$ were dissolved in chloroform and ethanol solution, respectively, and kept on stirring at 1000 rpm for 1 hour at room temperature (25ºC). The final active layer nanocomposite solution has been prepared by 0.5% wt/wt of silver nanoparticle in PBTTT-C14 solution. The channel becomes extremely conductive due to the larger concentration of silver nanoparticles in the pure polymer matrix, which is undesirable for the properties of transistors.

2.3 Device Fabrication

For the fabrication of the device, the following essential steps are to be followed.

- For wet cleaning purposes, a p-type doped Si wafer is treated with trichloroethylene and kept for ultrasonication for 5 mins.
- The substrate was then immersed in an isopropanol solution for five minutes, followed by three to four times rinsing through flowing deionized water (DI) water.

- Then piranha solution (H_2O_2:H_2SO_4 = 6:4) is used for the piranha cleaning treatment of the substrate by dipping the substrate in it for 20 min and subsequently washed with the running DI water 3-4 times. This piranha treatment with the substrate is performed to remove metal impurities, and organic impurities from the surface of the silicon wafer.
- Afterward, the wafer is dipped in HF in DI water solution (2-4 %) to discard the native oxide film from the surface of the substrate followed by 6-7 times treatment with running DI water. The wafer is dried at 100 °C in the presence of N_2 gas (N_2 ambient).
- The substrate dry cleaning was performed by plasma cleaning treatment in the presence of argon and oxygen gas (ratio 70:30) for 15 mins duration. Plasma cleaning forms an oxygen-rich hydrophilic surface, favorable for dielectric solution deposition.
- After performing the plasma treatment, proceeded for the spin-coating of zirconium acetylacetonate (ZAK) mixed strontium chloride solution over this Si (p++) wafer for the time interval of 60 seconds at 6000 r/min followed by the high-temperature annealing treatment of this coated film substrate in the presence of N_2 gas at 500° C for 2 hours for the growth of $SrZrO_x$ dielectric film.
- The resultant dielectric film is gone for the HMDS method which is vapor-based for 30 minutes to develop a hydrophobic substrate [129] over which the Organic Semiconductor (OSC) layer is to be deposited.
- The FTM technique has been opted for the development of OSC due to its cost-effectiveness, low wastage, and enhanced film growth technique. A detailed description has been given in [130], [131].

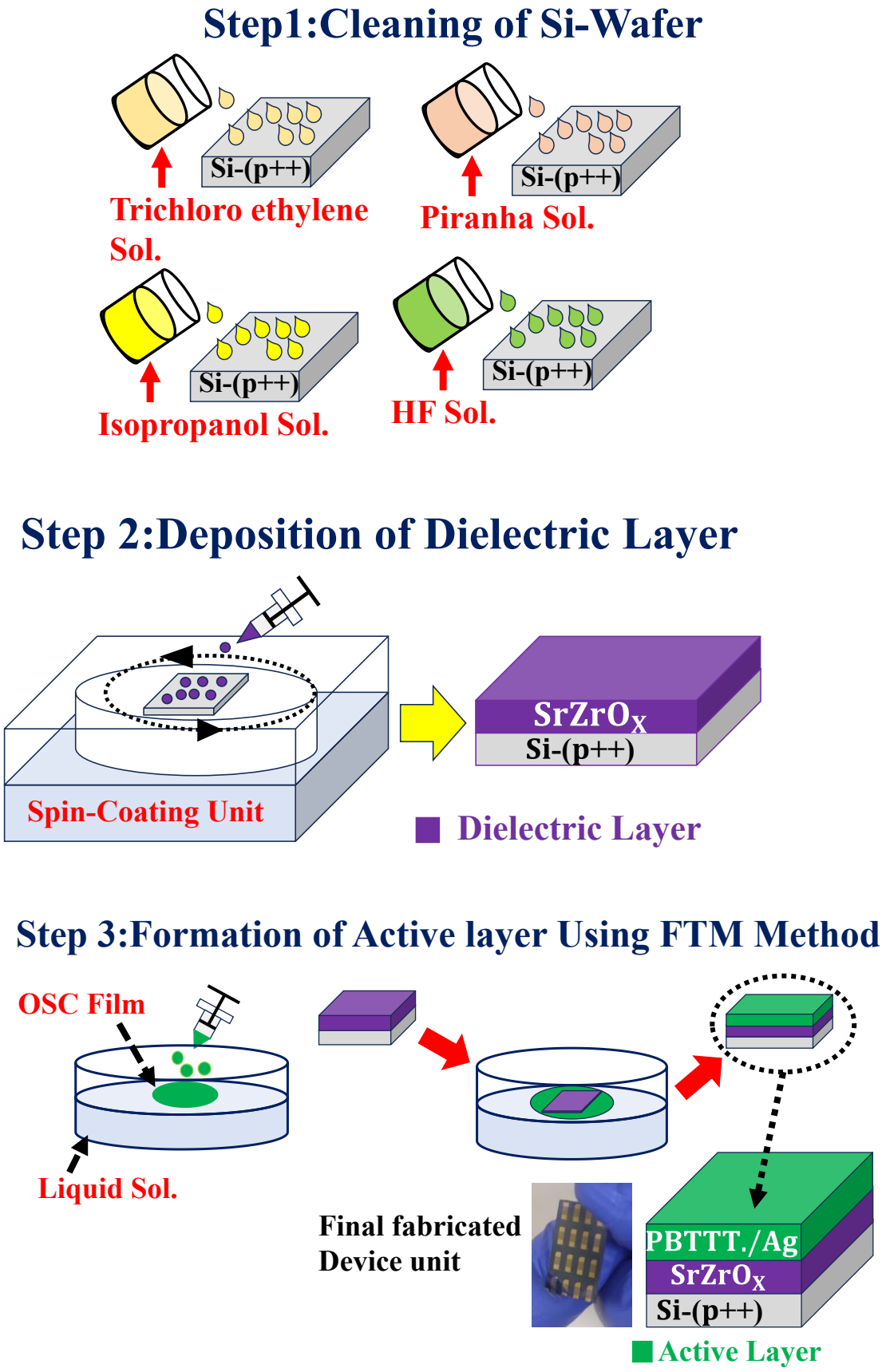


Figure 2.1 Showing the overview of different steps involved for device fabrication.

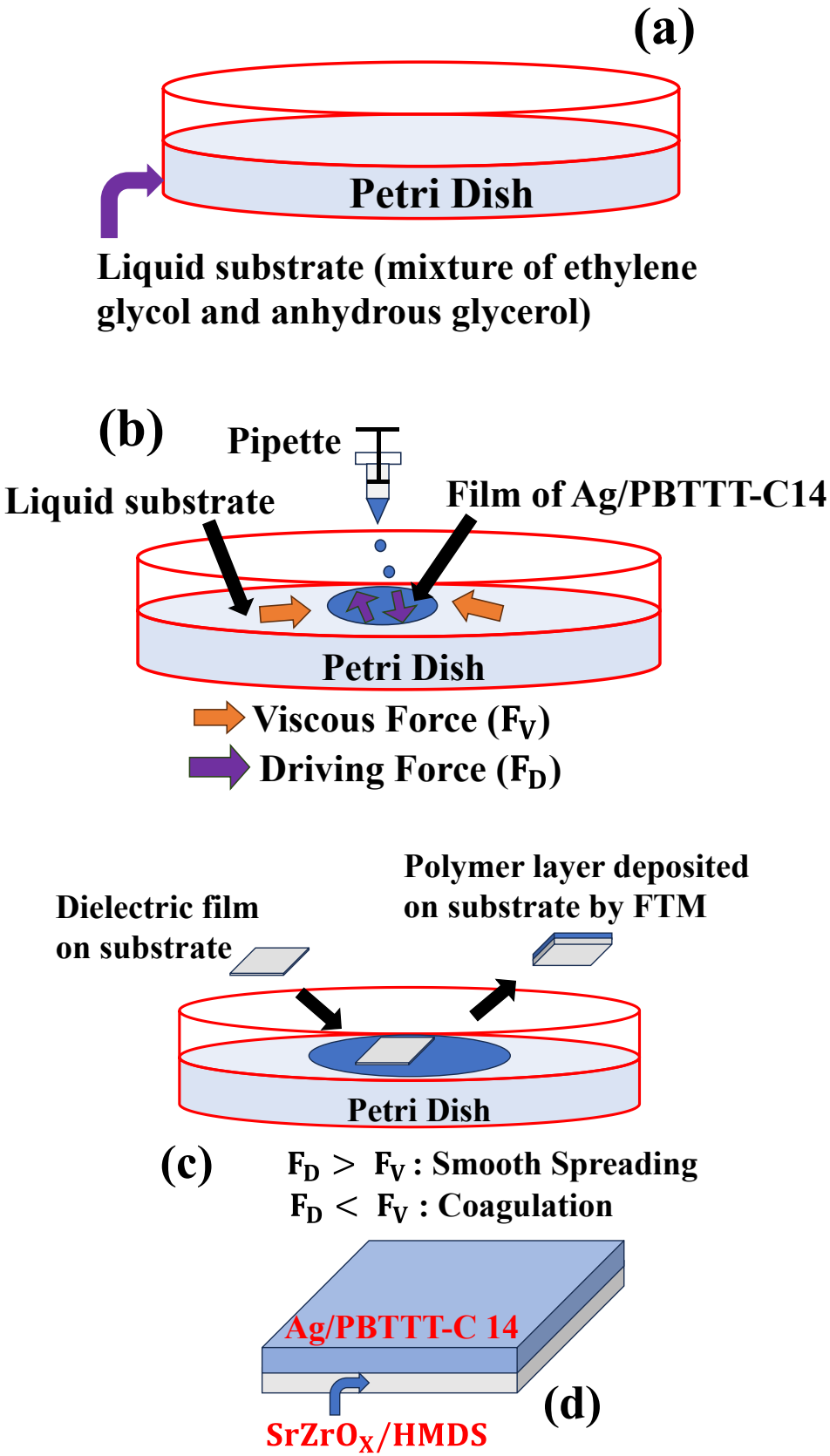


Figure 2.2 (a) Showing the liquid substrate poured into a petri dish (b) showing growth of thin film of silver nanoparticles doped PBTTT-C14 over a liquid substrate (c)

indicating the stumping of thin layer of silver nanoparticles doped Ag/PBTTT-C14 film over the HMDS treated dielectric film (d) showing uniform thin layer Ag nanoparticles doped PBTTT-C14 over dielectric film, acting as active layer of the OTFT.

For the development of an active layer (OSC) i.e., PBTTT-C14 by the means of FTM method can become possible when the surface energy magnitude of silver nanoparticles doped PBTTT-C14 is smaller than that of the liquid substrate (solution of Ethylene Glycol and Glycerol Anahydrous in 1:1). The following necessary steps are to be taken to obtain an active layer via FTM method.

Step 1: Liquid substrate exhibiting a high surface energy should be introduced by mixing ethylene glycol and anhydrous glycerol homogenously in the proportion of 1:1 and followed by pouring into the petri dish.

Step 2: Now, a drop (~10 μL) of silver nanoparticles-doped PBTTT-C14 dissolved in chloroform are dropped over the liquid substrate. As it possesses low surface energy as compared to the surface energy of the liquid substrate results in the growth of silver nanoparticles doped PBTTT-C14 and forms a thin and uniform floating film over the liquid substrate. In order to obtain smooth spreading, the driving force dominates viscous force in the film growth process i.e. ($F_D > F_V$) otherwise coagulation would take place which is undesirable for the film growth ($F_D < F_V$).

Step 3: Once, the formation of the thin and uniform floating film takes place then the floating film is stumped over the dielectric film (($SrZrO_x$) treated with HMDS) (Like water transfer process of painting) and annealed at 80 ºC for 3-4 hours for the removal of organic solvents residuals.

After this, to eliminate the leftover organic solvents annealing is done at 80°C. Gold is used for source and drain interdigitated contact of OTFT as shown in **Figure 2.3 (a)**,

having a width of 18.03 mm and length of 50 µm. The interdigitated contact of the device is deposited by thermal coating unit HHV 12A4D at ~10^{-6} torr pressure and 0.1 A°/sec rate. The thickness of dielectric film and active layer films are 60 nm and 30 nm respectively. The schematic of the device and fabricated image are shown in the **Figure. 2.3**

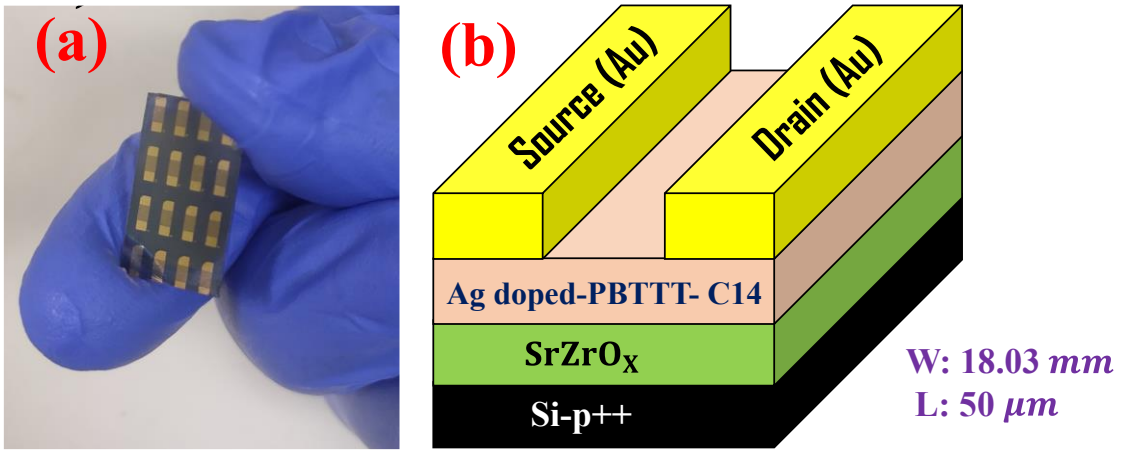


Figure 2.3 (a) Image of the fabricated device (b) Schematic of device illustrating different materials used in fabricating this device.

2.4 Thin Film Characterization

For the creation of an effective OTFT sensor, surface morphology analysis of the organic semiconductor film and dielectric film is become essential. A dielectric film of the device must pass with a smooth surface (surface roughness < 1 nm) so that it offers a good dielectric semiconductor interface. The active layer's development is controlled by a smooth dielectric film, and the device passes with high mobility because the interface between the dielectric and semiconductor is free of trapped charge carriers. The synthesized dielectric film in the current study satisfies the requirements for a good dielectric film with a low surface roughness of ~0.245 nm as depicted in (atomic force microscopy) AFM image of **Figure 2.4 (a) & (a')**. On the other hand, from AFM image

in the **Figure 2.4 (b) & (b')**, the silver-doped PBTTT-C14 has a surface roughness of ~1.102 nm and passes with a high value, providing active carrier sites for the adsorption of the gas molecules and, consequently, a strong sensing response.

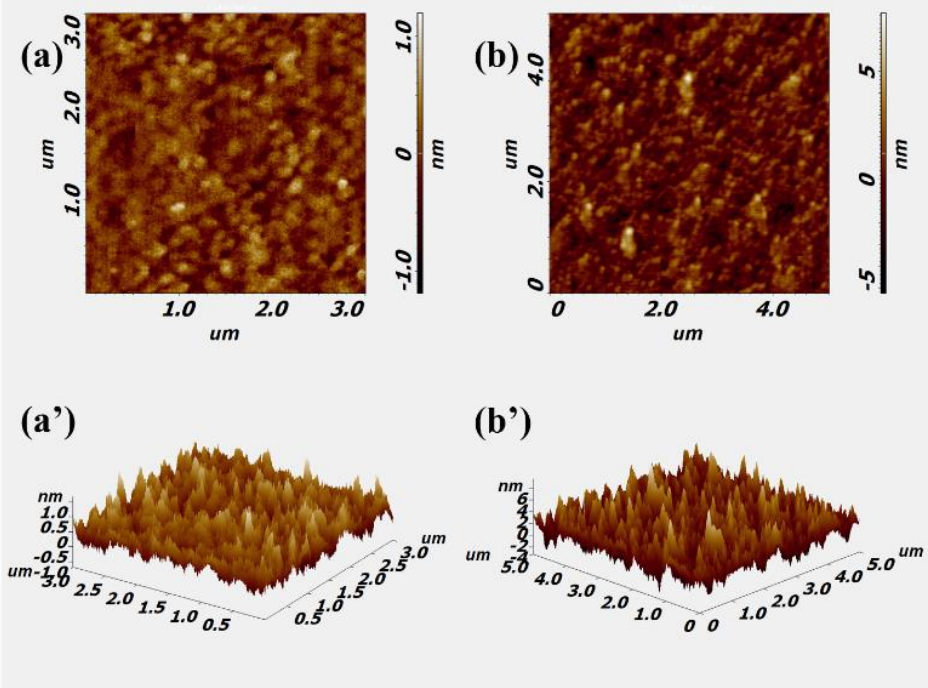


Figure 2.4 (a), (a') AFM images of SrZrOx film in 2D and 3D form, (b), (b') AFM images of PBTTT-C14/Au film developed over SrZrOx/HMDS film in 2D /3D form.

2.5 Dielectric Characterisation Results

A high-permittivity (κ) of dielectrics is one of the key parameters for realizing a high-performance and low-voltage OTFTs. These OTFT can be used either in sensing applications or switching applications due to consuming low power. In order to obtain the low operation voltage of OTFT in the range of 1V -3 V, the dielectric should have higher capacitive strength that hold the large amount of charge. The device configuration in the **Figure 2.5 (a)** was used to evaluate the capacitance of dielectric film, where dielectric film is sandwiched between gate (Si) and Au contact. The capacitance of the dielectric film is measured with respect to the frequency variation in **Figure 2.5 (b)** and it is observed that the dielectric film passes with the large areal dielectric capacitance of 433

$\frac{nF}{cm^2}$ at low operating frequency, which further validates the large no. of accumulated charge with low voltage.

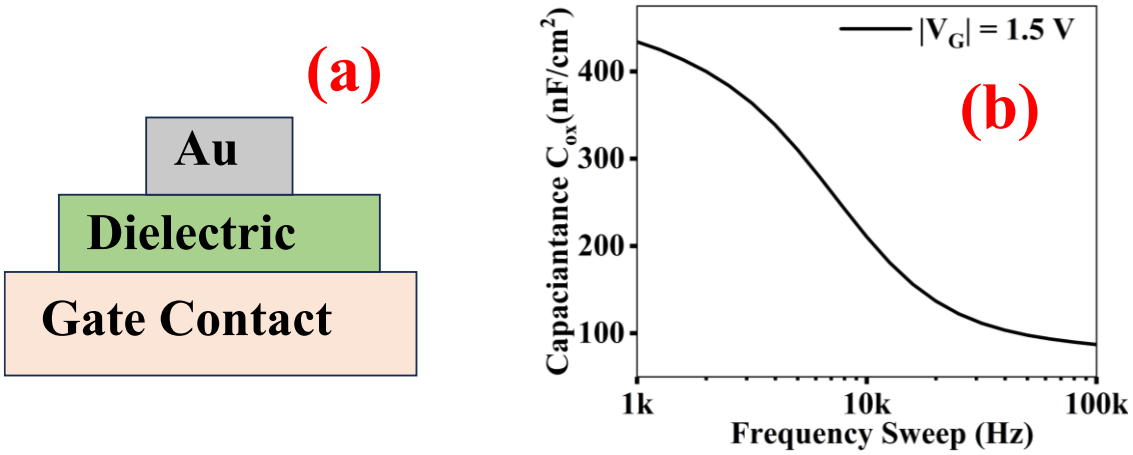


Figure 2.5 (a) Schematic for capacitance vs frequency measurement, (b) Capacitance vs frequency plot (C-f plot) of the manufactured dielectric film.

Another important parameter of dielectric is the leakage current density, a low leakage density is desirable for good dielectric. Therefore, to measure the strength of dielectric the leakage current density was measured and shown the plot in **Figure 2.6 (a)**. It is observed that the created dielectric film's has low number of pinholes. At a gate voltage (V_{GS}) of -1.5 V, the dielectric film has shown a low leakage current density of 0.1 nA/cm^2.

Additionally, UV Visible is performed through which absorbance versus wavelength curve is achieved, and according to the wavelength its corresponding bandgap is evaluated using the relation $E_g(eV) = \frac{1.24}{\lambda\,(\mu m)}$ then αhv is calculated using $\alpha hv =$ 2.303 × absorbance value × $E_g(eV)$, αhv is squared and curve $(\alpha hv)^2$ versus photon energy(hv) is plotted and the intercept of the curve on x-axis gives the bandgap of dielectric film which is obtained as 4.95 eV, as seen by the tauc plot in **Figure 2.6 (b)**. Further, the created dielectric layer has a band gap of 4.95 eV, which is sufficient tells to completely rule out the possibility of thermionic emission in the developed device.

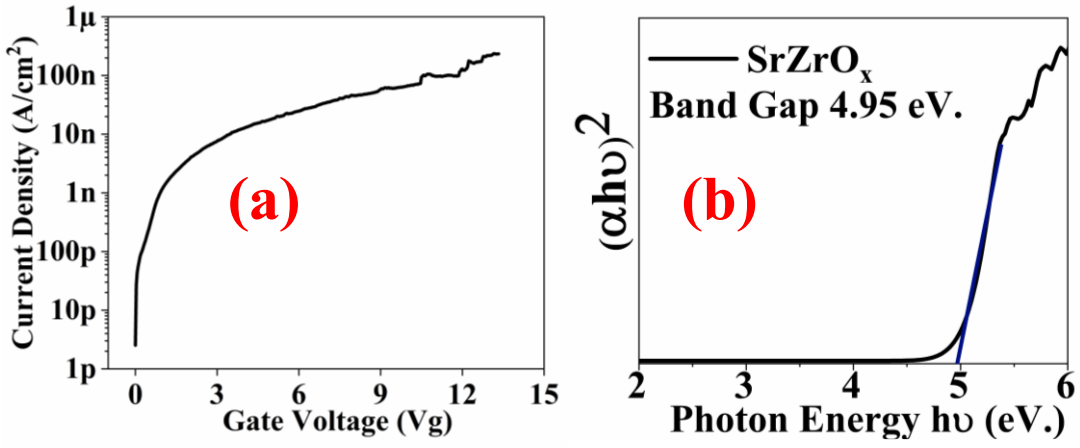


Figure 2.6 (a) Leakage current density plot of dielectric layer (SrZrOx) (b) Band gap of dielectric (SrZrOx).

2.6 Electrical Characterization Results

The output characteristics ($I_{DS} - V_{DS}$) of the fabricated device as shown in **Figure 2.7 (a)** has investigated for drain to source current (I_{DS}) with different drain to source voltage (V_{DS}) at different gate bias voltage (V_{GS}) from 0V to -1.5V with the step size -0.25. The maximum I_{DS} current of 3.5 µA is achieved at V_{DS} of -1.5 V at V_{GS} of -1.5 V. The output characteristics can further be divided into two important regions of operation i.e., 1. Linear region and 2. Saturation region. Generally, for sensing amplification, the device is used in saturation regions where the device's current is constant after particular V_{DS} . When the device is used in the saturation region, the drain current of this PBTTT-C14 based OTFT is defined by the equation (2.1).

$$I_{DS} = \mu_{SAT} \frac{W}{2L} C_{OX} (V_{GS} - V_{TH})^2 \qquad (2.1)$$

where μ_{SAT} is saturation mobility, C_{OX} is oxide capacitance, W and L is the width and length of a fabricated device. V_{TH} is the threshold voltage of the fabricated device. In the saturation region, the condition is $V_{DS} \geq V_{GS} - V_{TH}$.

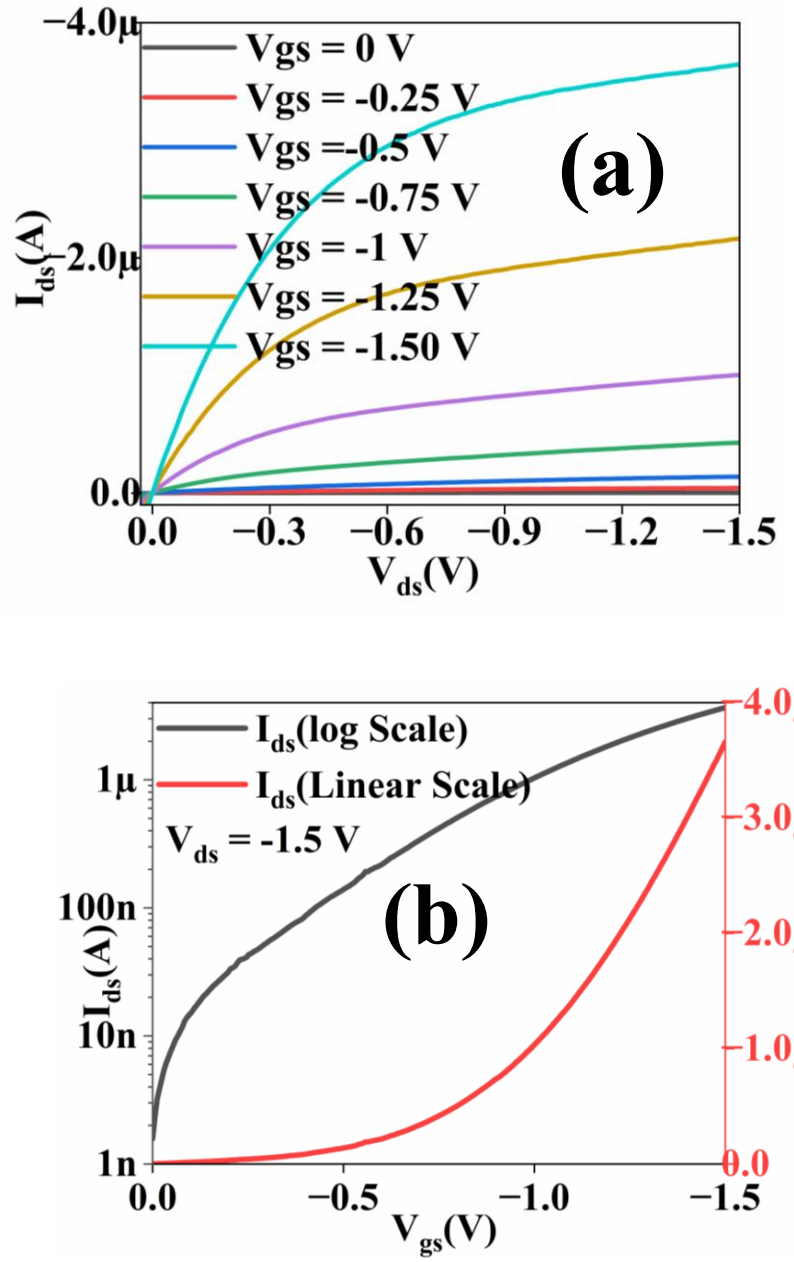


Figure 2.7 (a) Indicates output characteristics ($I_{DS} - V_{DS}$) curve for V_{DS} varying from 0 to -1.5 V with V_{GS} varying from 0 to -1.5 V with an increment of -0.25 V, (b) Indicates transfer characteristics ($I_{DS} - V_{GS}$) curve for fixed V_{DS} -1.5 V.

The characteristics indicate that the device can operate within a 1.5 V voltage, which is only made possible due to high-permittivity (κ) oxide dielectrics. The device parameters such as threshold voltage (V_{TH}), subthreshold swing (SS), on-off ratio (I_{ON}/I_{OFF}) and

saturation-mobility (μ_{SAT}) were extracted as -0.44 V, 0.5 $\frac{V}{Decade}$, 10^3 and 0.55 $\frac{cm^2}{Vs}$ respectively from the transfer characteristics of the device.

Table 2.1 Comparison of this OTFT with other existed TFT's

OTFT (Active layer)	**Deposition Technique**	V_{TH}/ **Op. V (V)**	μ ($\frac{cm^2}{Vs}$)	SS ($^V/_{decacde}$)	I_{ON} /I_{OFF}	**Reference**
P3HT	ALD	-1.2/ -5	0.01± 0.002	0.803 ± 0.243	10^4	[132]
Pentacene	Thermal evaporation	-2.9/ -10	0.4	1	3×10^4	[133]
DNTT	Vacuum Sublimation	-1/-3	1.3	-	10^6	[134]
C_{10}DNTT	Vacuum deposited	-7/-10	9.7	-	10^5	[135]
F8T2	Spin coating	-2/-6	1.69 ± 0.15	0.44 ± 0.05	10^4	[136]
Pentacene	Thermal evaporation	-1.1/ -6	0.4	0.2	10^5	[137]
PBTTT-C 14	FTM	-0.44/ -1.5	0.55	0.5	10^3	**This work**

2.7 Gas Sensing Results

To evaluate the sensing characterization of PBTTT-C14 based OTFT, the H_2S gas at different concentrations from 200 ppb (part per billion) to 5 ppm is exposed on the fabricated device in ambient conditions. The major parameters of OTFT such as mobility, threshold voltage, trap charge density, etc. are necessary factors to derive sensing findings, therefore, transfer characteristics ($I_{DS} - V_{GS}$) curve is used to evaluate all such parameters in the presence of H_2S gas. The $I_{DS} - V_{GS}$ characteristics as shown in **Figure 2.8 (a),** is obtained by varying the V_{GS} from 0 to -1.5 V at fixed V_{DS} of -1.5 V. In **Figure**

2.8 (a), it is noticed that, as H_2S gas concentration increases, it results in decay in the magnitude of drain current (I_{DS}). An increase in the concentration of H_2S gas over PBTTT-C14 based OTFT device may be due to the trapping of the charge carrier of the active layer by the molecules of the H_2S gas and an increment in the concentration of H_2S gas led to an increase in the level of trapping of charge carrier of organic semiconductor which results in a change in the value of (V_{TH}).This kind of behavior of (ΔV_{TH}) is previously observed for OTFT prepared by several others for marine, gas sensing applications[138]–[141]. The charges that trap in the channel of PBTTT-C14 are defined as Q_{TRAP} and its corresponding trap charge density (Δn) which is given in the following equations (2.2) and (2.3) [142].

$$Q_{TRAP} = \Delta V_{TH} C_{OX} \qquad (2.2)$$

$$\Delta n = {}^{Q_{TRAP}}/_{q} \qquad (2.3)$$

A subthreshold swing(SS) states the defect associated with interface and bulk [143]. SS depends upon the interface trap charge density, which is stated in the following equation (2.4) [144].

$$SS = \frac{KT}{q}\left(1 + \frac{q\Delta n}{C_{OX}}\right) \qquad (2.4)$$

where *K* stands for Boltzmann's constant, T for temperature, q for electronic charge, and C_{OX} for dielectric capacitance. It is worth noting that the H_2S is electron-donating gas and PBTTT- C14 is a p-type organic semiconductor, therefore when it is exposed to a p-type polymer, resulting in lowers charge density, the surface conductivity of the polymer and mobility[114], [128].

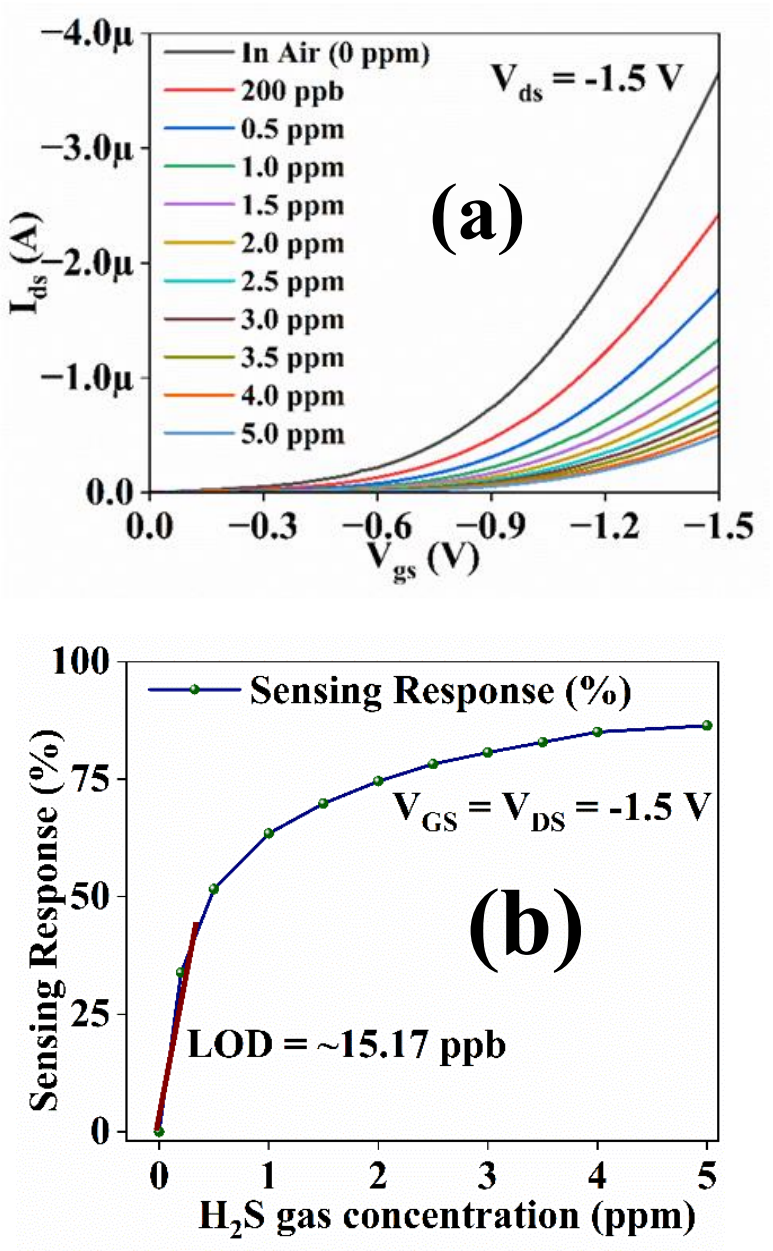


Figure 2.8 (a) Transfer characteristics ($I_{DS} - V_{GS}$) curve in the absence of the gas and in the presence of gas for variable concentration of H_2S gas carried out at a fixed value of V_{DS} = -1.5 V, (b) Showing sensing response at different concentrations of H_2S increasing from 0 to 5 ppm evaluated at $V_{GS} = V_{DS}$ = -1.5 V.

Further, the sensing response (S) of a gas sensor is another very essential and important parameter that describes the level of sensitivity of any gas sensor and it is defined by the following relation equation (2.5).

$$S = \frac{I_{DS(AIR)} - I_{DS(GAS)}}{I_{DS(AIR)}} \times 100 \qquad (2.5)$$

where $I_{DS(AIR)}$ is the drain current measured when H_2S gas is not present, and $I_{DS(GAS)}$ is the drain current measured in the presence of H_2S gas. It is seen that the calculated sensing response of this PBTTT-C14 based OTFT device is greater than 80 % at 5ppm of H_2S gas concentration as shown in **Figure 2.8 (b).** The Limit of Detection (LoD) of the fabricated gas sensor is obtained a 15.17 ppb, which is the well-permissible limit of good gas sensors.

It can also be illustrated that mobility (μ_{SAT}), threshold voltage (V_{TH}), and subthreshold swing (SS) change observed when H_2S gas is imposed on PBTTT-C14 based OTFT and its value and magnitude of μ_{SAT}, V_{TH}, SS decreases when the H_2S gas concentration exposure rises from 0 ppm to 5 ppm. **Figure 2.9 (a)** and **(b)** show what is happening at 0 ppm i.e., in the absence of H_2S gas the values of V_{TH} = -0.44 V and $\Delta n \sim 27\times 10^{13}$ cm^{-2}. As the concentration of H_2S gas varies from 0 to 5ppm and the corresponding value of Δn increases and V_{TH} decreases, hence it completely justifies the facts and cause mentioned above that increase in the gas concentration increases trapping of charge carrier of the active channel layer of the TFT device which decreases the (V_{TH}) threshold voltage of the device with an increase in the magnitude of threshold voltage in the negative region. It indicates that device on exposure to H_2S gas and increased concentration of gas from 0 to 5ppm required large amount of V_{TH} to turn ON the device. This is because of introducing of a large amount of charge trap densities results acting as a barrier in producing drain current [145].

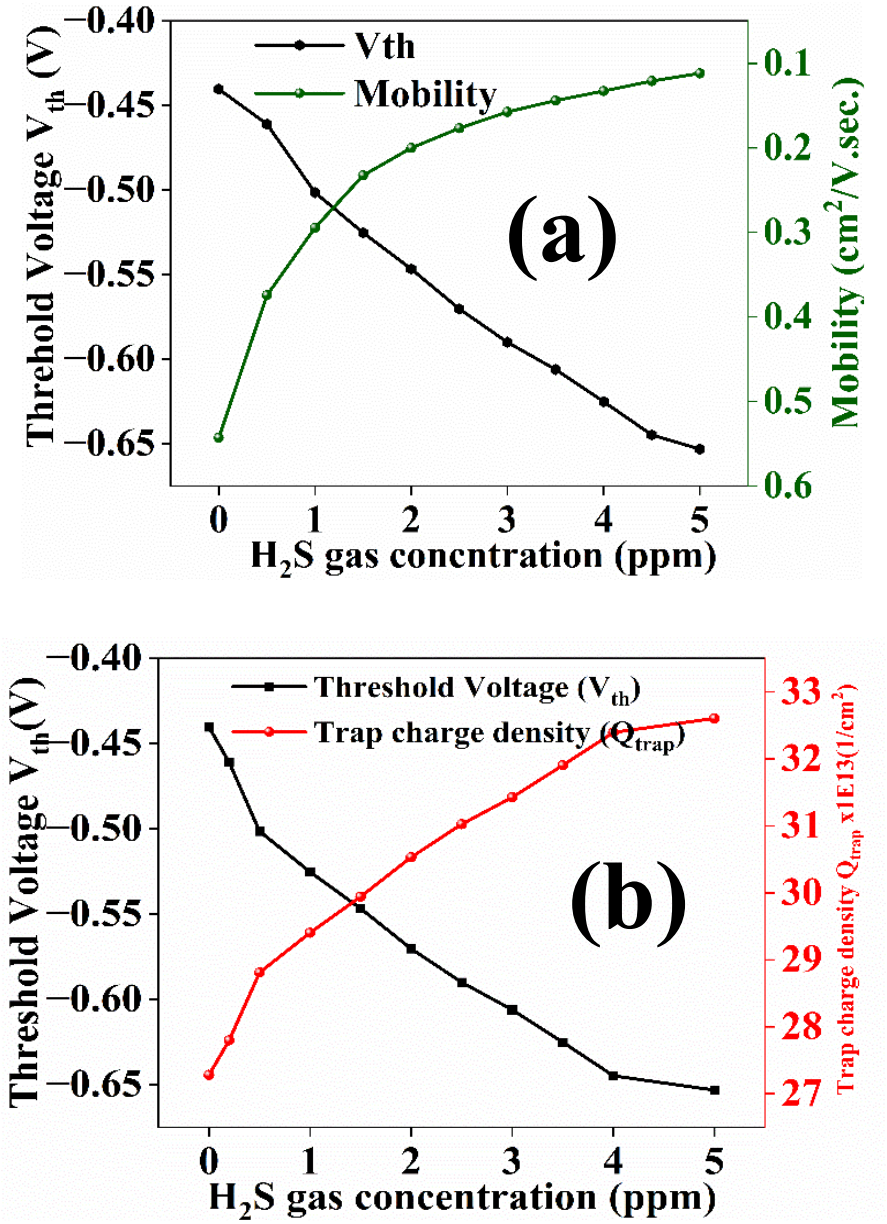


Figure 2.9 (a) Indicates a change in mobility (μ_{SAT}) and threshold voltage (V_{TH}) on exposure to H_2S gas for variable concentration from 0 to 5 ppm, (b) Stating change in the trap charge density(Δn), change in threshold voltage (V_{TH}) with an increase in the H_2S gas concentration.

As water molecule is polar in nature and it tends to induce the charge carrier of the organic semiconductor (OSC) as a result of which threshold voltage (V_{TH}), mobility (μ_{SAT}) got affected and reduced in the respective magnitudes due to interaction of charge carrier of

the active layer and polar water molecule. P-type OSC performance degrades when there is an increment in the levels of humidity[146], [147].

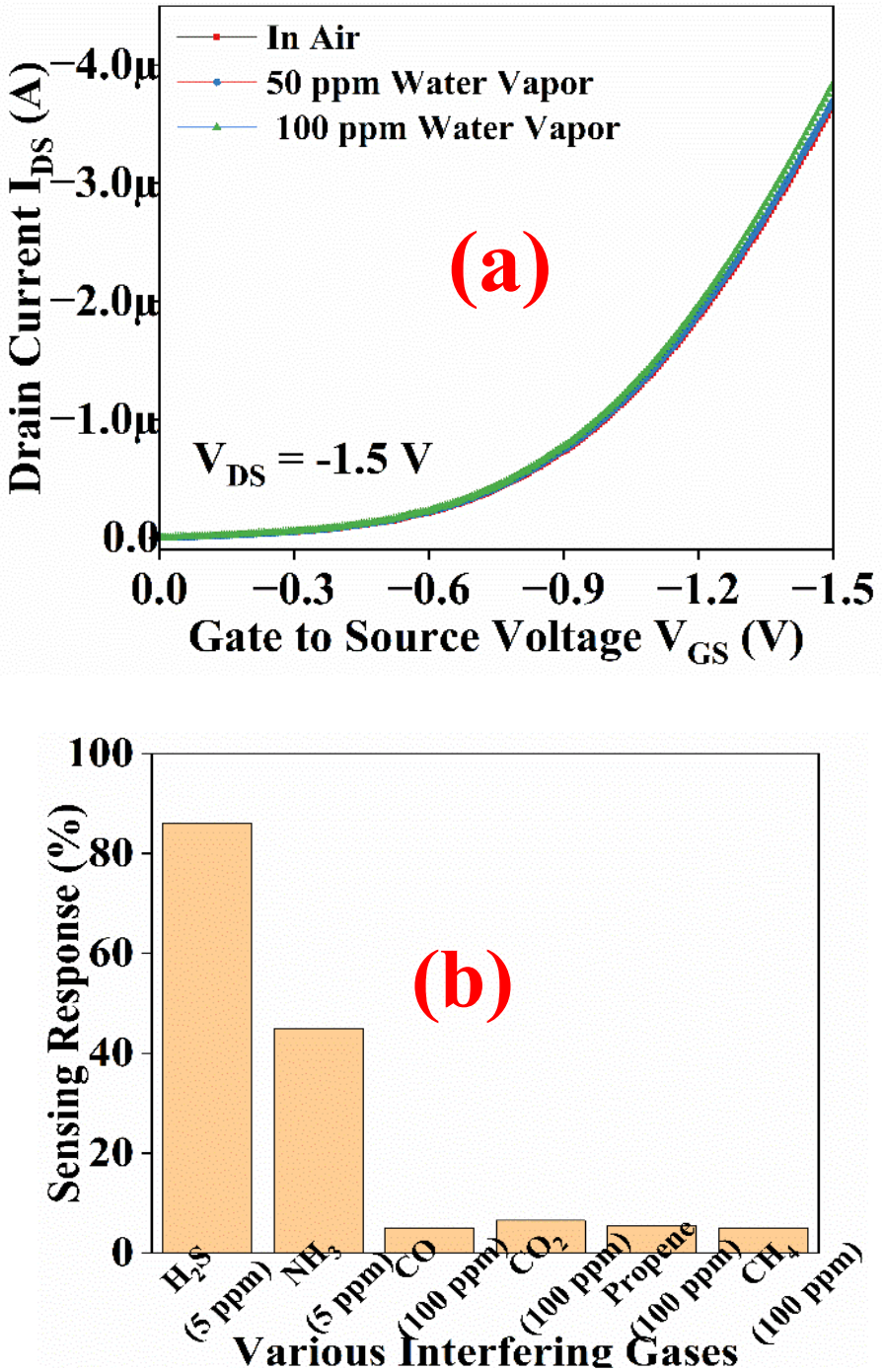


Figure 2.10 (a) Indicating transfer characteristics ($I_{DS} - V_{GS}$) curve at constant V_{DS} = -1.5 V for both the case in the presence of air only and for increase in the humidity condition, (b) Illustrating the nature of the sensing response for different interfering gases

carried out at different concentrations (H_2S, NH_3 - 5ppm, CO, CO_2, Propene and CH_4 – 100ppm).

In the current work, the device is almost independent of water vapors as shown in the **Figure 2.10 (a).** This is because of the introduction of metal nanoparticles in the organic polymer matrix forms a metal nanoparticle organic semiconductor nanocomposite matrix which eliminates the chance of water adsorption and desorption making it insensitive to the water molecules. The manufactured device has undergone selective analysis for various interfering gases, including H_2S, NH_3, CO, CO_2, propene, and CH_4 as illustrated in **Figure 2.10 (b).** From selective analysis results, it is justified that the fabricated gas sensor produces an excellent sensing response of > 80%, when subjected to H_2S gas and it can be now stated the device fabricated is fully favorable for sensing H_2S gas at RT

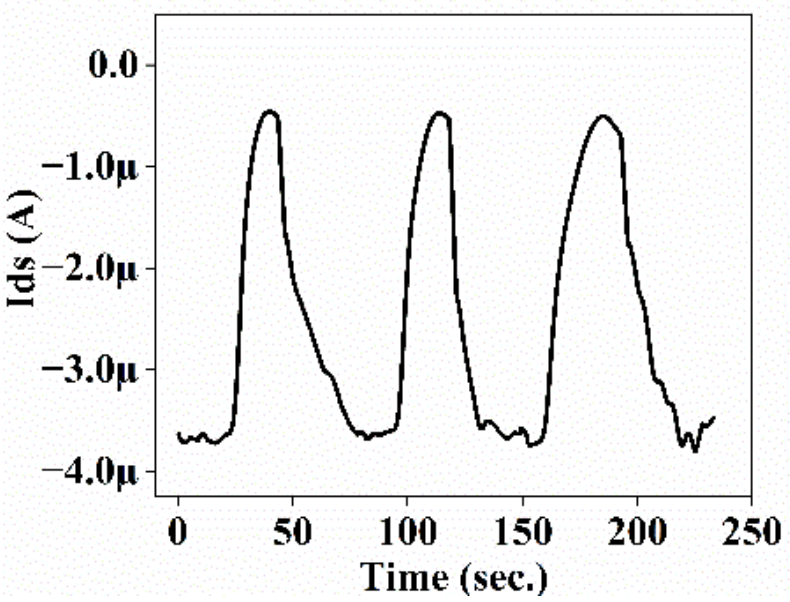


Figure 2.11 Showing the transient behavior and 3 repetitive cycles of the fabricated sensor evaluated at V_{DS} = V_{GS} = -1.5 V.

In order to evaluate the T_{Res} (average response time) and T_{Rec} (average recovery time) of the fabricated sensor, transient analysis is performed. Mechanism such as physisorption (surface based) or chemisorption (bulk based) over sensing surface are

linked for the determination of response and recovery time of gas sensors.

In this work, fabricated sensor highly favours physisorption over chemisorption mechanism and resulted in calculating T_{Res} and T_{Rec} as 5 and 26 seconds respectively. Additionally, from the **Figure 2.11** it indicates that 3 repetitive cycles of the proposed gas sensor.

Table 2.2 Comparison of this H_2S based sensors with other sensors

Sensor Type	**Sensing material**	**Deposition Technique**	**Sensitivity (%)**	**LoD**	T_{res} /T_{rec} **(s/s)**	**References**
Metal Oxide	WO_3	RF Sputtering	23 (1ppm)	1 ppm	30/30	[148]
Optical	Laser diode	Photoacoustic Spectroscopy	-	0.5 ppm	-/-	[149]
Electro-chemical	Nafion membrane	Spraying	2.92 (1 ppm)	0.1 ppm	9/-	[150]
OTFT	BTBT	Langmuir-Schaefer	15 (5 ppm)	60 ppb	40/>60	[151]
OTFT	PCPDTBT	FTM	71.3 (1ppm)	-	8/250	[152]
OTFT	PBTTT-C 14	FTM	80 (5ppm)	15.17 ppb	5/26	**This work**

2.8 Sensing Mechanisms

The sensing mechanisms of this PBTTT-C14 based OTFT have been explained in **Figure 2.12 (a)** and **(b)** respectively. In **Figure 2.12 (a),** explores the device in the absence of a target analyte, while **Figure 2.12 (b)** explores the interaction of the target analyte over the silver nanoparticle-doped sensing layer. The fabrication of the device's transfer characteristics (multi-parameter extraction) at the fixed drain to the source supply has been the subject of all sensing measurements. The doping and de-doping phenomenon

over the sensing surface of the metal-doped polymer nanocomposite sensing film can be used to explain the gas sensing mechanism of the manufactured sensor. It is well known that the PBTTT-C14 is a p-type organic semiconductor having large numbers of holes to modulate the drain current of the thin film transistor. The LUMO and HOMO of PBTTT-C14 are 3.2 eV and 5.1 eV respectively.

The work function of Au nanoparticle is 5.1 eV. Therefore, the difference between the work function of (Au) gold and HOMO is almost 0 eV.[153]–[155], This forms an ohmic contact results into no barrier for flow of charge carrier inside the semiconductor for the generation of drain current [156] and which would be further essential in evaluating all the performance parameters. When the sensing film of metal nanoparticles doped PBTTT-C14 interacted with the target analyte H_2S and ammonia, the lone pair of target gas trapped the active charge carriers in the sensing channel i.e., holes (indicated in **Figure 2.12 (b)**). In other words, the interaction of the target H_2S gas reduces the no. of active charge carriers (holes) in the channel by reducing the drain current of the fabricated organic TFT. The modulation of the drain current with the interaction of the target gas and sensing film resulting the sensing response of the sensor. When the gas from ambient has been removed, the sensor completely recovers to its initial state, confirming the dominant physisorption mechanism followed by the fabricated sensor. Additionally, the incorporation of the metal nanoparticles in the polymer matrix provides a high surface-to-volume ratio for the adsorption-desorption of gas molecules and enhances the sensor's sensing performance by donating the charge carriers over the backbone of the polymer matrix [157].

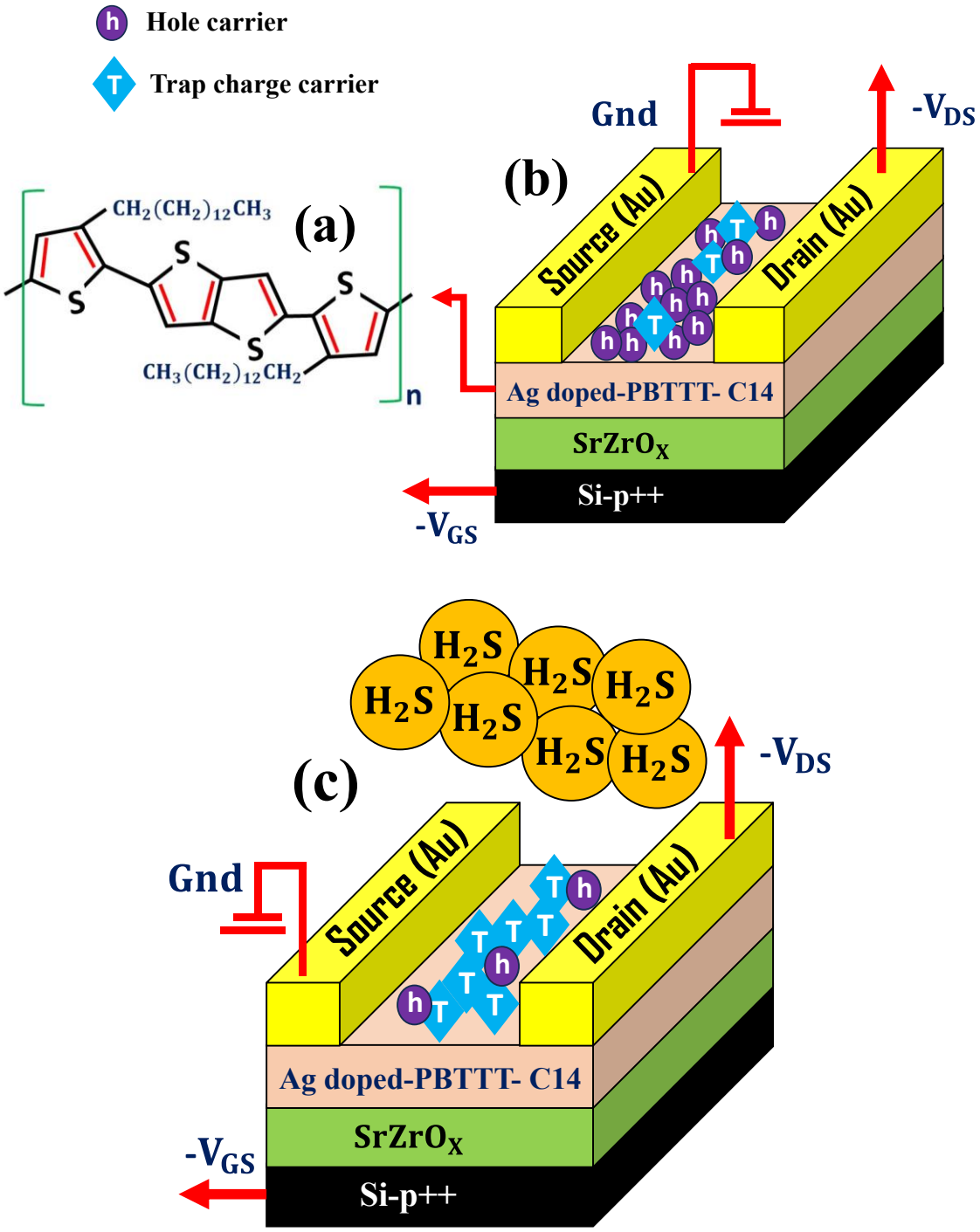


Figure 2.12 (a) Indicates PBTTT-C14 OTFT in the absence of H_2S gas, and (b) Indicates PBTTT-C14 OTFT when it is exposed to H_2S gas.

Due to the interchain transfer mechanism, the silver nanoparticles doping the polymer matrix improve the charge transport facility, which further cuts down on the target gas's

response and recovery times. Ag nanoparticles are also added to the polymer matrix to increase the catalytic activity, which enhances the sensor's sensing response in terms of response/recovery time.

2.9 Conclusion

The PBTTT-C14 based OTFT having top contact bottom gate structure has been fabricated for the detection of H_2S gas primarily for low value of concentration from 0 to 5 ppm. When the device is subjected to exposure of H_2S gas, it shows changes in the electrical behaviors. Also, it is found that an increase in the gas concentration increases the trap charge density of OSC, leading to an impact on the charge transport mechanism and resulting in enhancement in the sensing response. The sensing response is calculated, and found to be > 80 % at 5ppm. Along with H_2S gas, the device is subjected to various interfering gases and levels of humidity. All the aforementioned findings demonstrated that PBTTT-based OTFT has an excellent candidate for sensing H_2S gas.

Chapter 3

Compact Modeling of Flexible PBTTT-C14 Low-Voltage OTFT with PMMA/$SrZrO_X$ High-k Dielectric

3.1 Introduction

The last century was dominated by inorganic semiconductors including II-V, and II-VI materials. Even today silicon continues to rule the chip design industries. The beginning of the 21st century started witnessing the growth and widespread use of a new class of flexible and transparent electronics manufactured using organic Semiconductor-based OTFTs [158]–[160] . OTFTs have some interesting properties that are not shared by silicon-based transistors including the flexible and often transparent nature of the former, the ability to be manufactured virtually on any kind of substrate at or near room temperature, and sometimes without involving complex lithography techniques used in making Si-based transistors [161], [162] . A high operating voltage or power-hungry OTFTs are major constraints to meeting the demand of current low-power applications e.g., circuit and sensor applications [104], [132], [133], [163]–[165]. This is due to the fact that most of the high-k dielectrics are synthesized at higher temperatures [166], [167]. Thus most of the OTFTs are still fabricated on Si substrates resulting in a loosing of device flexibility [145], [168]. The ultimate aim of fabricated TFT is to utilize its fullest potential in IC design. Therefore, compact modeling becomes necessary for the development of prototypes of the circuits that are further utilized to demonstrate more complex circuit designs as per user demand and requirements. Researchers are facing challenges to those who fabricated OTFT devices in order to fit the behavior of the fabricated TFTs with models. This is due to the fact that the physical models are complex and time-consuming, and no such physical models are currently available to fit the

behaviour of all these new TFT devices due to the variation of material properties, different device structures, and fabrication process variability. Researchers are using pre-existing standardized SPICE compact models to fit the TFT behaviours, however, these models may be accurate for limited regions of operation [93], [169], [170]. Thus, to fill the gap of both shortcomings as discussed in aforesaid statements, this chapter demonstrated the fabrication of an OTFT device at low temperatures in ambient conditions preserving device flexibility with good device parameters. Further, this chapter mainly addresses modeling issues for new TFT devices through a fast and innovative compact modeling approach. The active layer of fabricated device is developed by the means of floating film transfer method (FTM) which is cost efficient, small amount of solution wastage and provides uniformity in film thickness [171], [172].

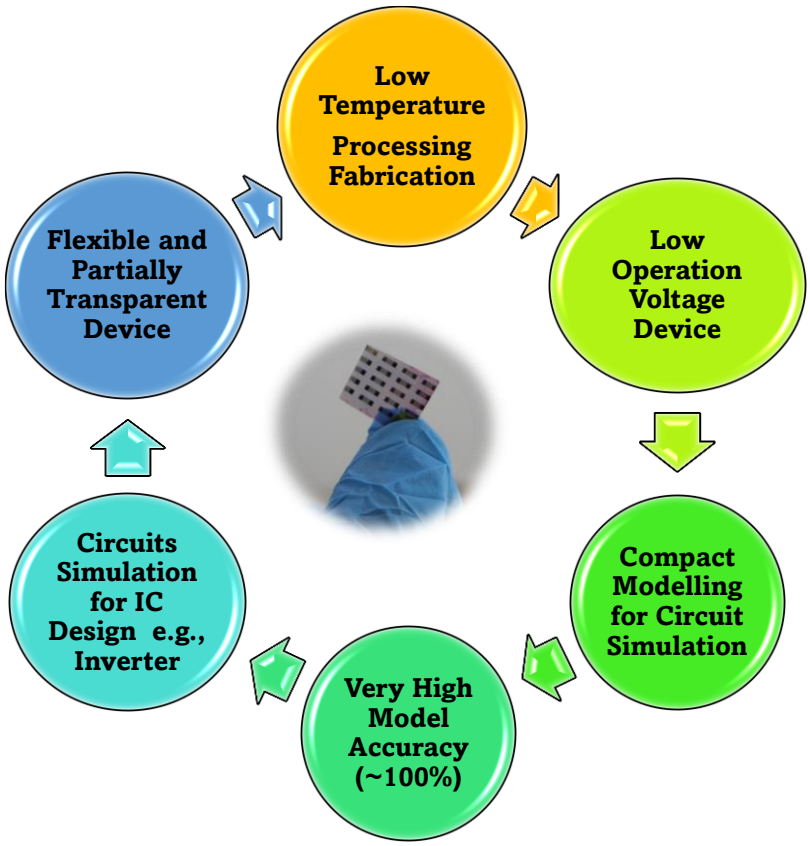


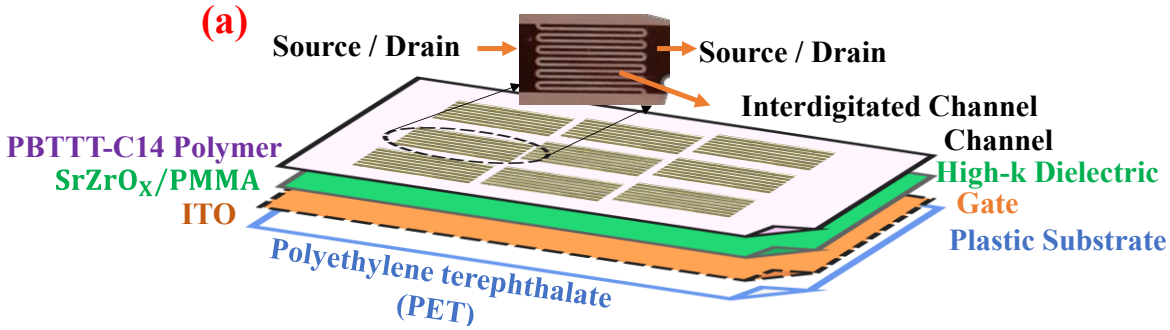
Figure 3.1 Showing the overview of this paper and different steps involved for device fabrication and circuit simulation.

3.2 Chemical Required and Materials Synthesis

PMMA (Poly Methyl methacrylate) (MW- 350k), Strontium chloride, Zirconium (IV) acetylacetonate (ZrAc), 2MEA (2 Methoxy Ethanol), and other cleaning agents and organic were purchased from Merck India Pvt. Ltd. The dielectric solution 300 mM of SrCl2 ,100 mM of ZrAc solution and and 80 mg/ml of PMMA were dissolved separately in 2-MEA solution and kept on constant stirring at 900 rpm and Room Temperature (RT) for 3 hours. Subsequently, the strontium chloride solution and ZrAc solution were mixed in a separate vial tube for the preparation of SrZrOx solution and further kept on constant stirring at 900 rpm and RT for 3 hours. The ratio of the strontium chloride and ZrAc solution has been optimized with a ratio of 1:6 (wt/wt) for smooth, high dielectric constant and high band gap dielectric film. Further, the PMMA solution was mixed with SrZrOx solution in a ratio of 20:80 for the synthesis of the final PMMA blend SrZrOx solution for dielectric film fabrication. For the active layer solution, 10 mg of PBTTT-C14 was dissolved in 1 ml of chloroform and stirred for 1 hour at RT at 900 rpm for uniform mixing solution.

3.3 Device Fabrication

The bottom gate – TFT device have been fabricated consisting of different layers is depicted in the **Figure 3.2 (a)**.



The device has exhibit both partially transparency and flexibility as shown in device image respectively in the **Figure 3.2 (b-b''') and (c).**

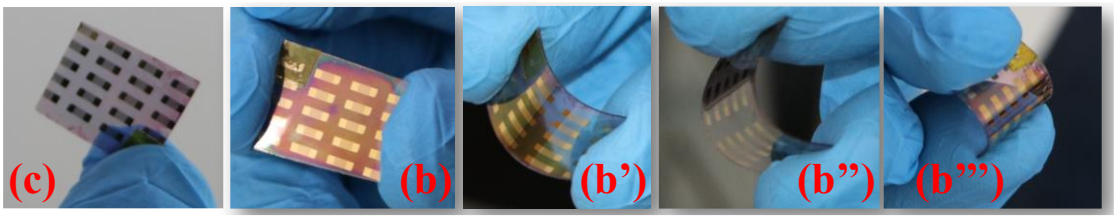


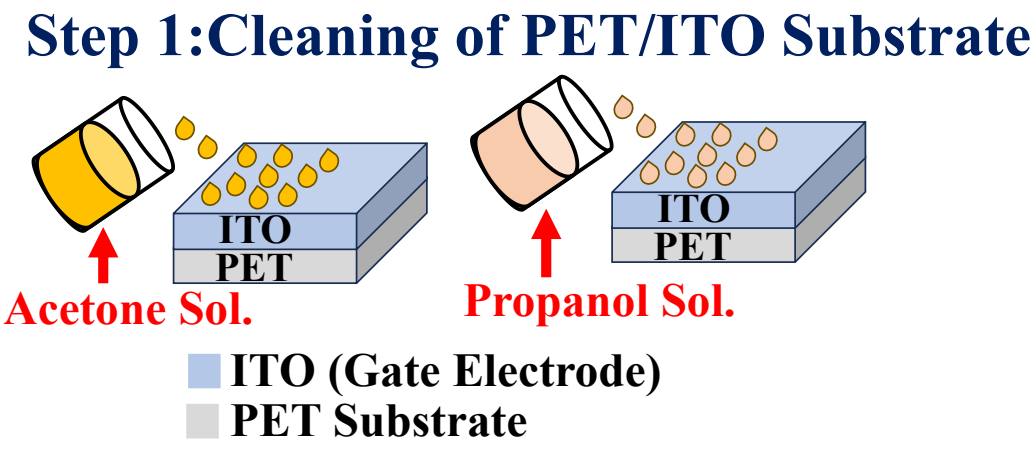
Figure 3.2 (a) Schematic of the device showing different layers of fabricated device are the images of the fabricated device (b) (b') (b'') (b''') Image showing flexibility of device (c) Transparency.

The following necessary steps were used for fabricating the low operating voltage of flexible and transparent thin film transistor:

- **Step 1:** Initially, indium tin oxide (ITO) coated PET substrate (15×10 mm) is treated with each acetone and propanol for 10 mins respectively, after that it was washed with deionized water (DI) water.
- **Step 2:** The cleaned ITO coated PET substrate was it kept in oven to get dried at 80℃ in the existence of N_2 gas for 10-15 min followed by the plasma cleaning for the duration of 10 minutes to enable the surface oxygen rich which is feasible for the growth of dielectric solution over it.
- **Step 3:** After plasma cleaning, with the help of spin coating method (SPM-200), the dielectric layer of polymethyl methacrylate (PMMA) blend $SrZrO_X$ over gate electrode is deposited over ITO followed by pre-annealing at 70℃ for the duration of 20-24 Hours. PMMA blend $SrZrO_X$ are mixed in volume-wise proportion of 20:80 for enhancing mechanical flexibility without losing the high-k properties.
- **Step 4:** After pre-annealing, the UV-Visible treatment is done for the duration of 15 minutes separately for both UV and Visible treatment respectively.
- **Step 5:** After this UV-Visible treatment, the dielectric film over the substrate was kept on thermal chuck (80 ºC) for treating with vapor form of Hexamethyldisilane

(HMDS) for the time interval of 20 minutes. This HMDS treatment helps making the surface hydrophobic in nature and also minimizes the associated interface traps for the film growth of organic semiconductor (OSC) on gate dielectric [129].

- **Step 6:** For the active/organic film growth Polyethene glycol and glycerol are added in homogenous proportion of 1:1 and stirred it nicely to form the liquid solution. The PBTTT-C14 in chloroform solution has been taken for the floating film transfer method (FTM), detailed process of FTM method is given in [130]. A 20 μl drop of obtained metal doped polymer nanocomposite solution was poured at surface of liquid substrate (Polyethene glycol and glycerol) solution for the active layer growth of the film.
- **Step 7:** After that film was stumped over the HMDS cured dielectric film and baked at 70℃ to 80℃ for 5 hours to get a uniform active layer film. The film thickness of the active layer measured by Filmetrics F20-UV at various places is known as 30±3 nm.
- **Step 8:** A 50 nm gold were used to deposit the source and drain contact with a width of 18.23 mm and channel length of 50 µm by thermal coating unit HHV 12A4D at ~10^{-6} torr pressure and 0.1 A°/sec rate.



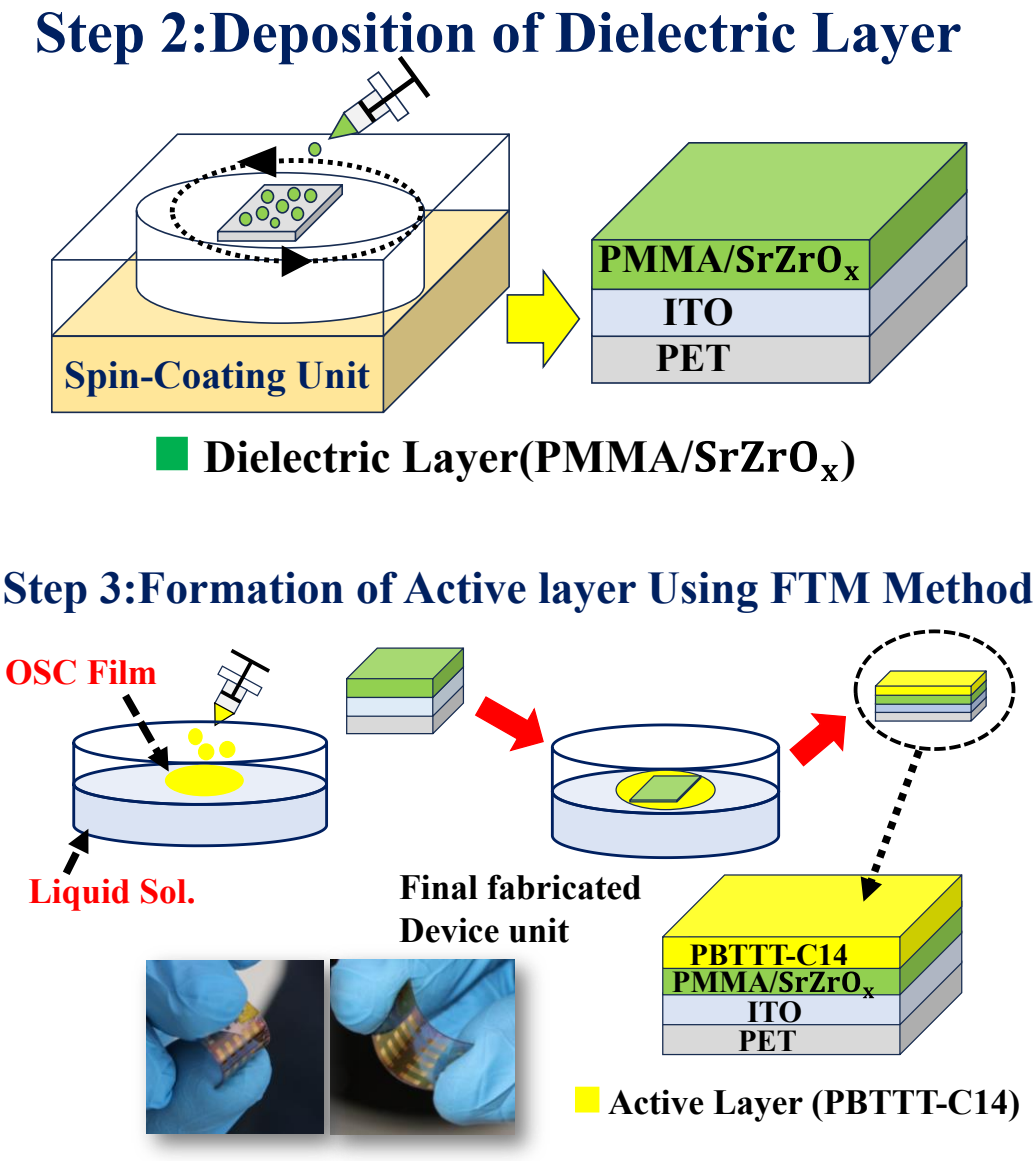


Figure 3.3 Showing the overview of different steps involved for device fabrication.

3.4 Thin Film Characterization

The flexibility of the device has been performed on a cylindrical setup. The device's operation is satisfactory up to 10 mm bending radius. For a high bending radius, the device characteristics are destroyed but the device is recoverable when the bending stress is removed. For the function of OTFT, active layer and dielectric plays a crucial role for its functioning and operation. Therefore, analysis of surface morphologies is essentially required for the fabrication of transistors.

To achieve a good semiconductor dielectric interface, surface roughness of dielectric film should be < 1nm. Smooth dielectric thin film helps in controlling the establishment of active layer of OTFT and having good interfacing properties i.e., negligible trapping of charge carries between the interface of semiconductor and dielectric, results into high mobility of the device [173]. **Table 3.1** presents the variations in surface roughness and dielectric constant with respect to the ratio of PMMA and $SrZrO_X$. The optimized ratio of PMMA and $SrZrO_X$ has been determined for device based on the data, ensuring that the surface roughness remains well below 1 nm. The AFM (atomic force microscopy) using Model: NTEGRA Prima Company: NT-MDT Service & Logistics Ltd. has done to obtain the surface roughness of the deposited dielectric film as shown in the images of **Figure 3.4 (a) and (b).** The result states that the obtained surface roughness of dielectric (PMMA $SrZrO_X$) and active layer films are 0.407 nm and 1.273 nm respectively, confirms good dielectric film exhibiting low surface roughness with excellent interface properties and large no. of active sites are present on the active layer film of organic semiconductor.

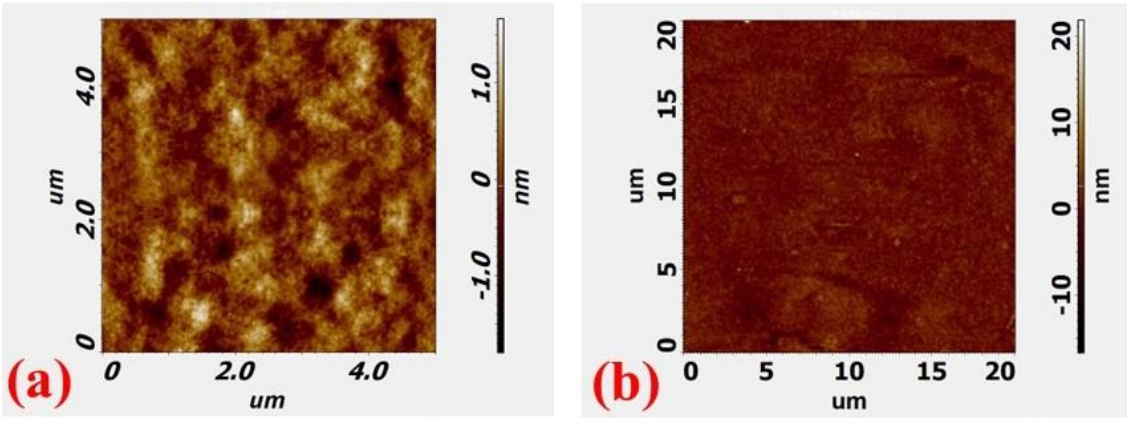


Figure 3.4 (a) AFM image of $SrZrO_X$: PMMA film in 2D form (b) AFM image of Au/PBTTT-C14 film established over $SrZrO_X$: PMMA/HMDS film in 2D form.

Table 3.1 Surface Roughness and Dielectric Constant as Function of PMMA: $SrZrO_x$ Ratio of Dielectric Thin Film

Sr No.	PMMA: SrZrOx Ratio	Roughness	Dielectric Const.
1	0:100 (Pristine SrZrOx)	1.037 nm	~32.2
2	20:80	0.407 nm	~31.44
3	30:70	3.2 nm	~31
4	40:60	10.41 nm	~28

3.5 Dielectric Characterisation Results

To ensure the low voltage operation and high-performance, could achieved by the proper utilization of dielectric layer in the TFT device which possess high-k dielectric value to solve the shortcoming of battery hungry devices. Dielectric exhibiting higher value of capacitance is an important key for achieving low operating voltage OTFT having voltage (1-2 V) as high capacitance have holding strength for large number of charge carrier.

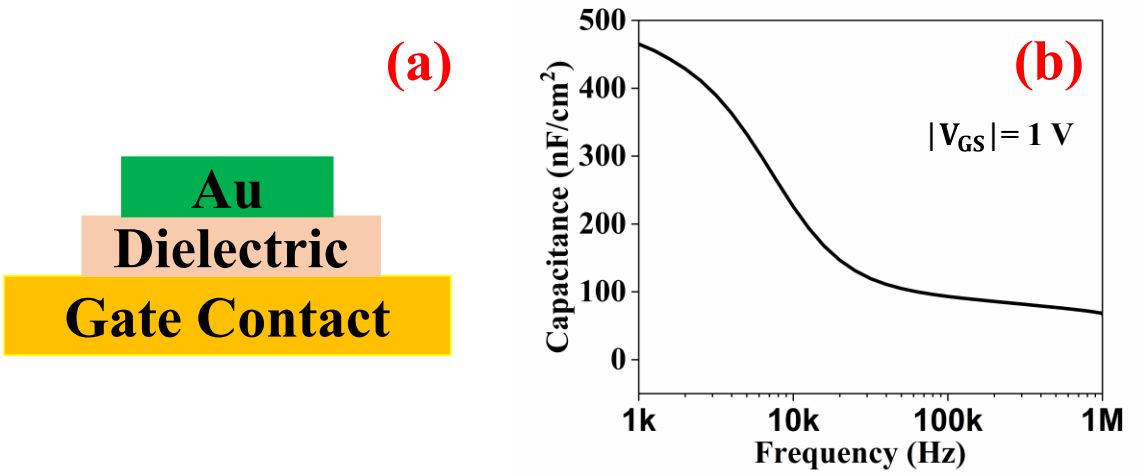


Figure 3.5 (a) Device schematic used to measure the capacitance vs frequency curve (b) Capacitance vs frequency curve(C-f) plot of dielectric film formed for the fabricated device.

In **Figure 3.5 (a)** the device with different layers where dielectric is situated in between metal contact (Au) and gate contact (ITO) for determining dielectric capacitance has been characterized by Semiconductor Parameter Analyzer B1500A. From **Figure 3.5 (b)** it can

be noticed that the capacitance vs frequency plot, dielectric capacitance evaluated at low frequency is 464 $\frac{nF}{cm^2}$ confirms that dielectric is capable enough for the accumulation of large number of charges carrier at low voltage. As the average thickness of the dielectric film (d) is calculated as 60 nm measured by Filmetrics F20-UV at various places. After that the dielectric constant (k) can be determined with the help of **Figure 3.5 (b)**. Therefore, value of (k) is calculated using $C_{OX} = (\varepsilon * k)/d$ formula, and found of 31.44, that confirms high-k dielectric is utilized in device fabrication. Along with capacitance vs frequency curve, leakage current density is obtained that determines the strength of dielectric film.

For a good dielectric film lower value of leakage current density is desirable which can be noticed in plot of **Figure 3.6 (a)** that states the leakage current density is observed 10 nA/cm^2 at V_{GS} = -1 V, supports that no availability of pinholes.

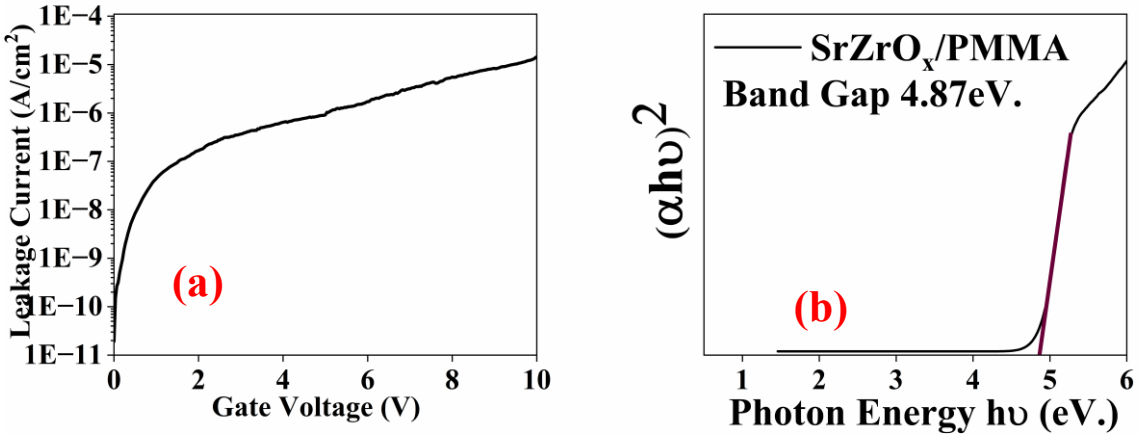
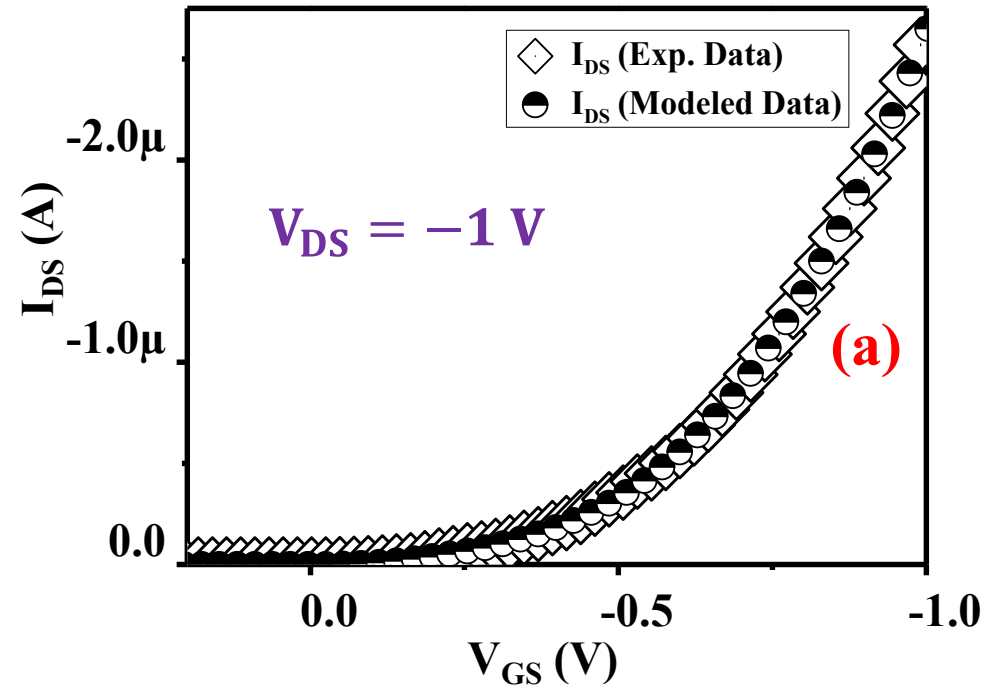


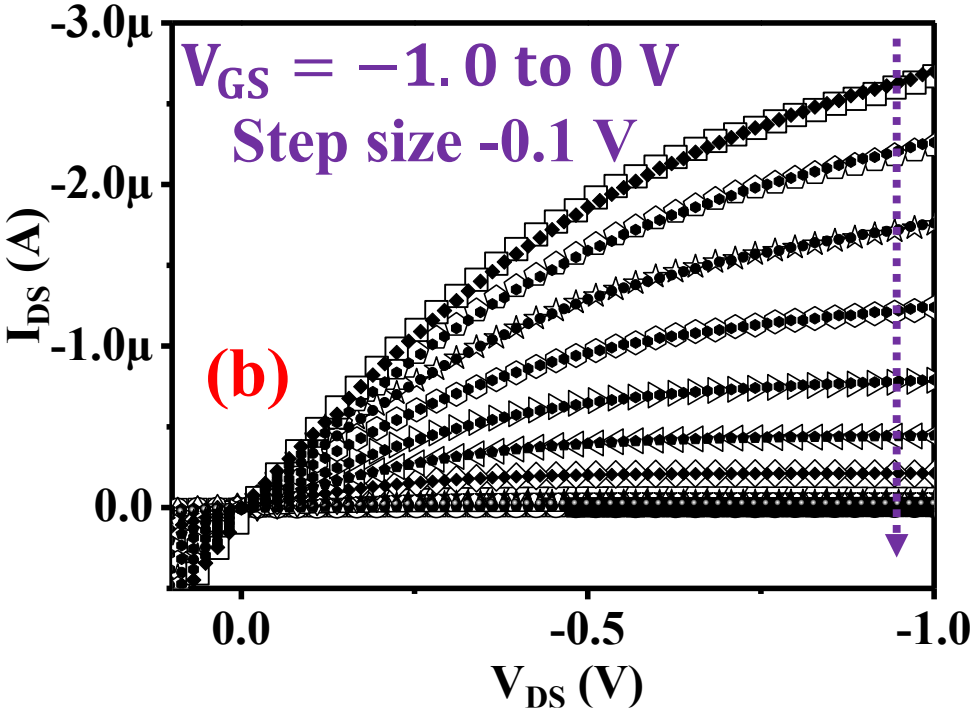
Figure 3.6 (a) Leakage current density curve of dielectric ($SrZrO_X$/PMMA) (b) Bandgap of dielectric film ($SrZrO_X$/PMMA) formed for the fabricated device.

The high bandgap of 4.87 eV is calculated for the hybrid dielectric film which is evaluated with help of tauc plot as seen in **Figure 3.6 (b)**, describes that the fabricated device would

eliminate the possibility for thermionic emission. The band gap of the dielectric film has been measured by JASCO V-700 UV/Vis. spectroscopy.

3.6 Electrical Characterization Results





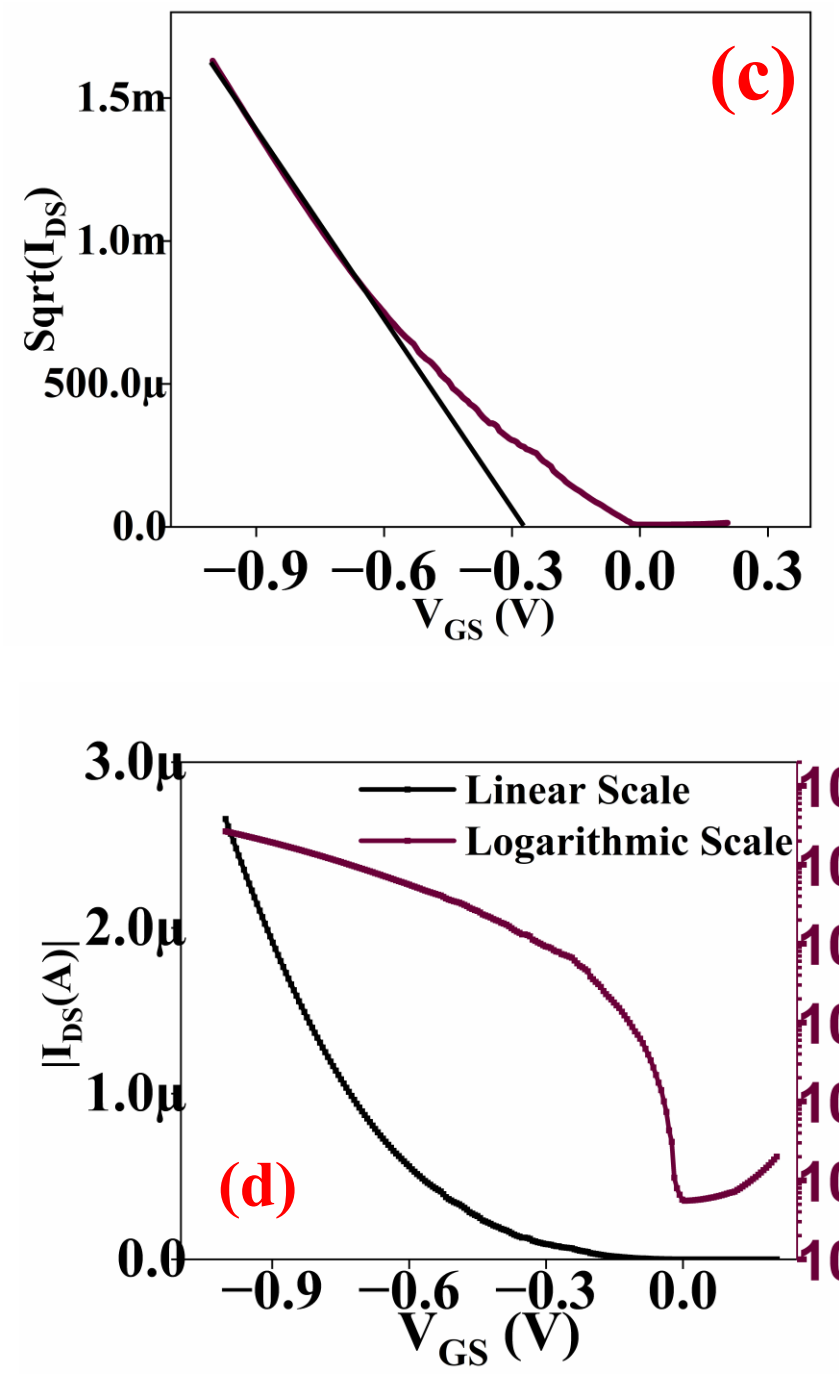


Figure 3.7 (a) Comparison of experimental and modeled data of transfer curve i.e., Drain current – Gate to Source Voltage $(I_{DS} - V_{GS})$ (b) Output characteristics curve i.e., Drain current – Drain to Source Voltage $(I_{DS} - V_{DS})$ for Gate voltage (V_{GS}) varying from 0 to -1V having step size of -0.1 V. (c) ($\sqrt{I_{DS}} - V_{GS}$) curve for evaluating the threshold

voltage (V_{TH}) (d) Logarithmic curve (log (I_{DS}) $- V_{GS}$) for estimating on-off ratio (I_{ON}/I_{OFF}) and subthreshold swing (SS).

In this work, TechModeler device modeling tool from Silvaco has been used for compact modeling of fabricated low voltage flexible and partial transparent OTFT devices. It is observed that the comparison of measured experimental results (performed by Semiconductor Parameter Analyzer B1500A) of both transfer and output drain characteristics of OTFT with modeled results shows excellent compatibility with model accuracy of above 99%. In this modeling approach of compact modeling in which percentage (%) of error is estimated corresponding to the numbers of iterations (data values)[174] and superimpose of experimental data and modeled data observed in **Figure 3.7 (a) and 3.7 (b)** confirms that its corresponding error is very small which is 0.37% and 0.74% respectively. Plots of transfer and output characteristics curve seen in **Figure 3.7 (a) and (b)** shows that the operating voltage of this device is -1.0 V which becomes possible because of utilizing dielectric film providing higher areal capacitance shown in **Figure 3.5 (b)**. Transfer curve ($I_{DS} - V_{GS}$) is plotted for V_{GS} varies from 0 to -1 V at fix V_{DS} = -1 V. Similarly for output curve V_{DS} varies from 0 to -1 V for variable V_{GS} from 0 to -1 V with an increment -0.1 V. When PBTTT-C14 based device operated in saturation mode then drain current equation (3.1) becomes as follows

$$I_{DS} = \mu_P \frac{W}{2L} C_{OX}(V_{GS} - V_{TH})^2 \qquad (3.1)$$

For a device to be operated in saturation mode or region, drain-source voltage should be equal or greater than difference between gate-source voltage and threshold voltage respectively. Where μ_P is refer to the hole mobility, C_{OX} is refer to the oxide capacitance, W and L are the width and length of device respectively. V_{GS}, V_{DS} and V_{TH} are gate-source

voltage, drain-source, and threshold voltage of fabricated device. **Figure 3.7 (b)** shows that at fix V_{GS} = -1.0 V, the saturated drain current is observed as -2.68 μA. With the help of **Figure 3.7 (c) and (d)** the value of all performance parameters as threshold voltage (V_{TH}), subthreshold swing (SS), on-off ratio (I_{ON}/I_{OFF}) and hole mobility (μ_P) are calculated as -0.272 V, 0.2 $\frac{V}{Decade}$, 0.5×10^5 and 0.06 $\frac{cm^2}{Vs}$.

Table 3.2 Comparison of OTFT Device Parameters

OTFT (Active layer)	**Deposition Method**	**V_{TH}/ Op. V (V)**	**$\mu\left(\frac{cm^2}{Vs}\right)$**	**$SS\left(V/dec.\right)$**	**I_{ON}/I_{OFF}**	**Remark [References]**
Pentacene	Thermal evaporation	-2.9/ -10	0.4	1	3×10^4	High operating voltage and high SS value [133]
TIPS-Pentacene	Inkjet Printing	-1.2/ -60	0.02	2.52	10^4	Very high operating voltage [104]
C8-BTBT	Spin Coating	-3/ -15	18.3	-	1.5×10^5	High operating and threshold voltage, although excellent mobility of channel is acheived [175]
C_{10}DNTT	Vacuum deposited.	-7/ -10	9.7	-	10^5	High temp processing have been used for channel deposition, although high operating voltage, with good channel mobility [135]
F8T2	Spin coating	-2/-6	1.69 ± 0.15	0.44 ± 0.05	10^4	Low temperature processing for channel deposition, along with good TFT parameters [136]
PBTTT-C14	FTM	-0.27/ -1	0.06	0.2	10^5	Low temperature processing fabrication, fully flexible, Low operating voltage, low SS value, low mobility, with good On-OFF ratio **[This work]**

The stability and precision of the device were assessed by conducting tests on 20 fabricated devices with a substrate area of 1.5 cm × 2 cm. The findings showed minimal

variance. In **Table 3.2,** All the performance parameters of fabricated OTFT are compared with the existing TFT's. **Table 3.3** shows the fabrication technology information of 20 devices and lists the statistical variations of TFT parameters.

Table 3.3 Process Technology Parameters

No. of Device Tested = 20	V_{TH} (V)	$\mu\left(\frac{cm^2}{Vs}\right)$	$SS\left(V/_{dec.}\right)$	$\nabla V_{TH-hystersis}= V_{TH-forward} - V_{TH-Backward}$
Mean	0.27	0.06	0.2	0.0150
St. devi:	0.017	0.009	0.024	0.0013

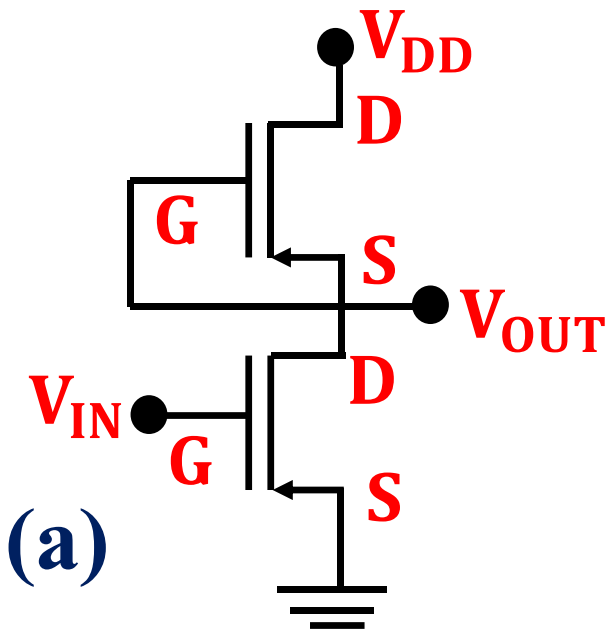
3.7 Compact Modeling and Inverter Circuit Simulation

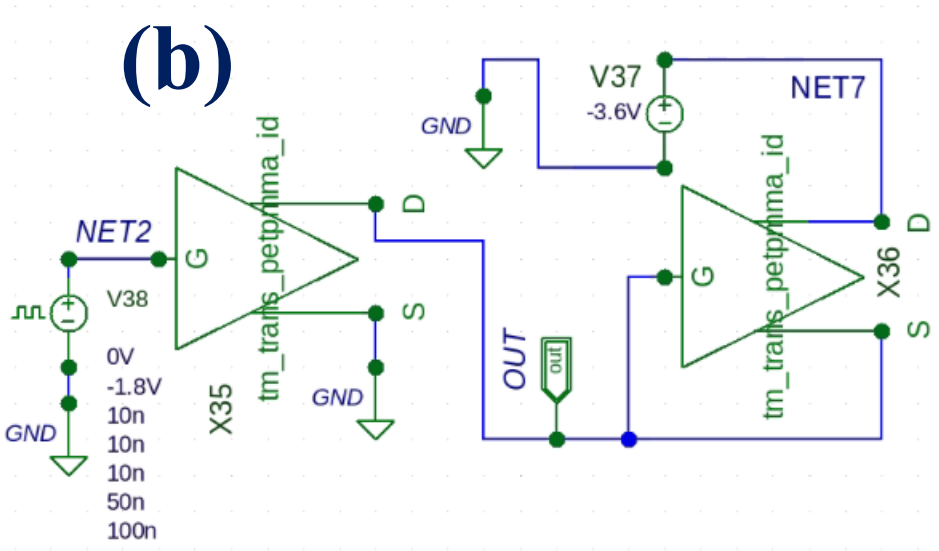
With help the Silvaco-Techmodeler tool, device compact modeling is done and along with modeling experimental data, smart-spice file are also generated that can be used for the circuit simulation[174]. From this P-TFT (PBTTT-C14 based OTFT), we have implemented drive-in load inverter circuit on Silvaco-Gateway platform whose detailed description are shown as follows:

- Current Voltage (I-V) characteristics measured from the fabrication of P-TFT (PBTTT-C14 OTFT) device are loaded to the Silvaco-Techmodeler tool
- From this I-V measurement, P-TFT model has been opted. In the modeling section, % of error is estimated corresponding to the number of iterations. When the modeling reaches 100%, modeled data is generated according to the data supplied to Silvaco-Techmodeler tool
- This P-TFT model is further imported further analysis and realization of circuits.
- At Silvaco-Gateway tool all types of analog and digital circuits are implemented, in this tool basic libraries exist which contain components such as vpulse, vdd,

gnd, etc. In addition to this, Smart-Spice simulator also exist in Silvaco-Techmodeler tool which is used to check transient and voltage transfer characteristics.

- For the simulation of an inverter circuit, from this model (.sp) file is imported at Silvaco-Gateway platform for circuit implementation and using smart-spice simulator transient and voltage transfer characteristics has been observed to estimate parameters such as propagation delay, voltage gain.





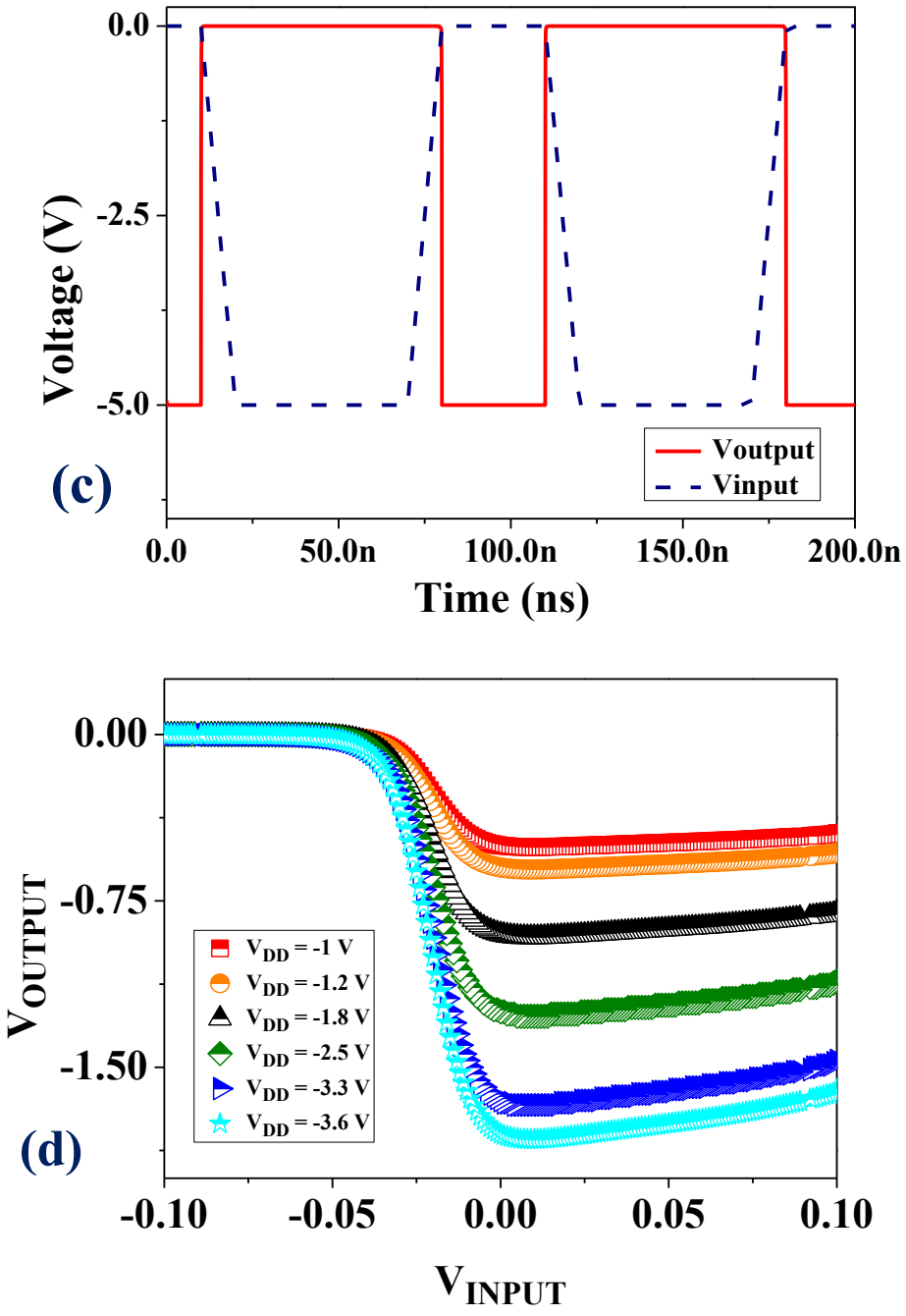


Figure 3.8 (a) Schematic diagram of drive-in load inverter circuit implemented using PBTTT-C14 OTFT (b) Implementation of inverter circuit at gateway platform. (c) and (d) Showing the transient behavior and voltage transfer characteristics of inverter circuit.

For this drive-in load inverter circuit, two P-type OTFT are utilized in the circuitry. a zero-gate source load configuration is chosen for realizing the inverter circuit, as this

topology provides high gain and high logic swing. The entire inverting behavior of the inverter circuit can be realized based on the input of the driver OTFT [37]. The schematic of drive-in load inverter zero gate source load configuration is shown in **Figure 3.8 (a)** and **Figure 3.8 (b), (c) and (d)** show circuit implementation in gateway platform and its corresponding transient curve and voltage transfer curve.

Table 3.4 Showing DC Inverter Gain at Different V_{DD}

Case Number	V_{DD} (V)	Gain (V/V)
1	-1.0	10.68
2	-1.2	13.11
3	-1.8	19.6
4	-2.5	29.7
5	-3.3	36.3
6	-3.6	39.77

Table 3.5 Comparison of Different Inverters

Inverter Material	Channel Deposition method	Operating Voltage (V)	Gain (V/V)	Reference (Remark)
P3HT-co-PEGT	Spin coating	1 V	10.3	Moderate gain ,complex fabrication[176]
N1450/P3HT	Spray Printing	60 V	17	Very high Operating voltage[177]
PBTTT/N1400	Inkjet Printing	20 V	4.4	High Operating voltage and very low gain [178]
diF-TES-ADT/ TU-3	Inkjet Printing	2.5	14	Low operating voltage, moderate Gain[179]
MoS_2/Rubrene	CVD/ Physical vapour transport method	3.3 V	2.3	Low operating voltage and very low gain [180]
PBTTT-C14	FTM	3.6 V	39.77	Low operating voltage and high gain **[This work]**

The transient analysis helps in calculating parameters such as propagation delay high to low (τ_{PHL}) = 61ns, propagation delay low to high (τ_{PLH}) = 9 ns and average propagation delay (τ_{PD}) = 35 ns respectively. From, **Figure 3.8 (d)** the gain of this inverter is evaluated to its corresponding voltages that are mentioned in **Table 3.4**, low-voltage CMOS operated at voltage -1.2 V, -1.8 V, -2.5 V, -3.3 V, -3.6 V specified in this[181]. The gain of different inverters are compared with this fabricated one is shown in **Table 3.5**.

3.8 Conclusion

The fabricated PBTTT-C14 based OTFT exhibits flexible as well as bending nature, the operating voltage is -1 V which is very small and the performance parameters calculated as on-off ratio (I_{ON}/I_{OFF}) ~ 0.5×10^5, hole mobility (μ_P) of 0.06 $\frac{cm^2}{Vs}$, subthreshold swing (SS) ~ 0.2 $\frac{V}{Decade}$ confirms high on current and faster switching from off state to on state. Additionally, experimental data verified using techmodeler-silvaco tool, illustrating small error (0.37% and 0.74%), circuit simulation is also performed on gateway platform showing the voltage gain of ~39.77 at V_{DD} = -3.6 V. From all above facts mentioned above confirms that this OTFT fabricated on PET substrate have excellent bending properties and applicable for low voltage application.

Chapter 4

Fully Transparent and Flexible Low-Voltage a-IGZO TFT for Full Adder and Full Subtractor Circuit Design

4.1 Introduction

In recent years, it has been noticed and observed that transparent amorphous oxide semiconductors (TAOS) are highly preferred over transparent oxide semiconductors. Among different examples of TAOS, a-IGZO (amorphous-indium gallium zinc oxide) exhibits excellent properties such as high mobility, a wide band gap, and stable amorphous characteristics. a-IGZO contributes high mobility with a higher order magnitude as compared to a-Si and organic semiconductors. The wider bandgap of a-IGZO-based TFT (~3.25 eV) contributes to small leakage across the channel as compared to a-Si: H-based TFT because it consists of a narrow bandgap of ~1.1 eV. This wider band gap is helpful to obtain good off-state drain current leakage characteristics. [182]–[184]. This amorphous nature provides excellent film uniformity and device-to-device consistency over large areas—an essential requirement for high-resolution display backplanes and flexible electronic systems. The amorphous structure also enables low-temperature fabrication (<300°C), which is compatible with flexible polymer substrates such as PET and PI. a-IGZO exhibits high electron mobility (10–20 $cm^2/V \cdot s$), which is significantly higher than that of amorphous silicon (a-Si:H) and comparable to or even better than polycrystalline ZnO [185], [186]. While ZnO offers simplicity and relatively low cost, it suffers from unstable carrier concentrations and grain boundary scattering, leading to device instability. In_2O_3, though possessing higher intrinsic mobility, is prone to oxygen deficiency, resulting in poor threshold voltage stability [187]. The incorporation of indium (In) provides a broad conduction band derived from In 5s

orbitals, ensuring good electron transport even in the amorphous phase. The presence of gallium (Ga) in the IGZO composition plays a crucial role in controlling oxygen vacancies, which are the dominant donor defects in oxide semiconductors. Gallium atoms form stronger bonds with oxygen, thereby suppressing excessive free carriers and improving bias-stress stability and threshold voltage control. Zinc (Zn) contributes to the film's amorphous stability and helps maintain balanced conduction and structural integrity [188]. Several constraints exist, such as gate-bias stress, gate-illumination stress, gate-temperature stress, etc., which cause the instability of a-IGZO and finally impact the device performance [189]–[191]. Therefore, in the past years, different approaches and techniques have been used and adopted in order to improve the performance of a-IGZO-based TFT, such as variable active layer thickness, different compositions of In:Ga:Zn, the formation of active layers using sputtering, partial oxygen pressure, plasma treatment, etc., the implementation of passivation layers, the employment of different-k values of insulators such as SiO_2 (silicon dioxide), Si_3N_4 (silicon nitride), Al_2O_3 (aluminum oxide), etc. But these approaches seem very complex and costly in nature [192]–[197]. Among various types of gate insulators, high-k dielectric (ZrO_2, HfO_2, etc.), i.e., k > 15, is preferred over SiO_2 to avoid gate leakage current caused by quantum tunneling. This leakage current is highly impacted by the degradation of TFT performance [126], [127], [198]–[201]. Recently, for the high performance of IGZO-based TFT, several methods, such as the ultraviolet-assisted oxygen ambient rapid thermal annealing method (UR-ORTA) and electrospun highly aligned IGZO nanofiber array in which $HfAlO_X$ is utilized as a high-k dielectric, were opted for due to the high-order magnitude of mobility ~ 23.12 and 15.9 $\frac{cm^2}{Vs}$ [202], [203]. In the previous reported work, fully transparent TFTs have been developed but have high operating voltages of 40V and 20V and exhibit poor

performance parameters such as subthreshold slope (SS) ~ 371 $^{mV}/_{decade}$, threshold voltage (V_{TH}) ~ 21 V, mobility (μ) ~ 7.4 $\frac{cm^2}{Vs}$,etc [204]–[206].

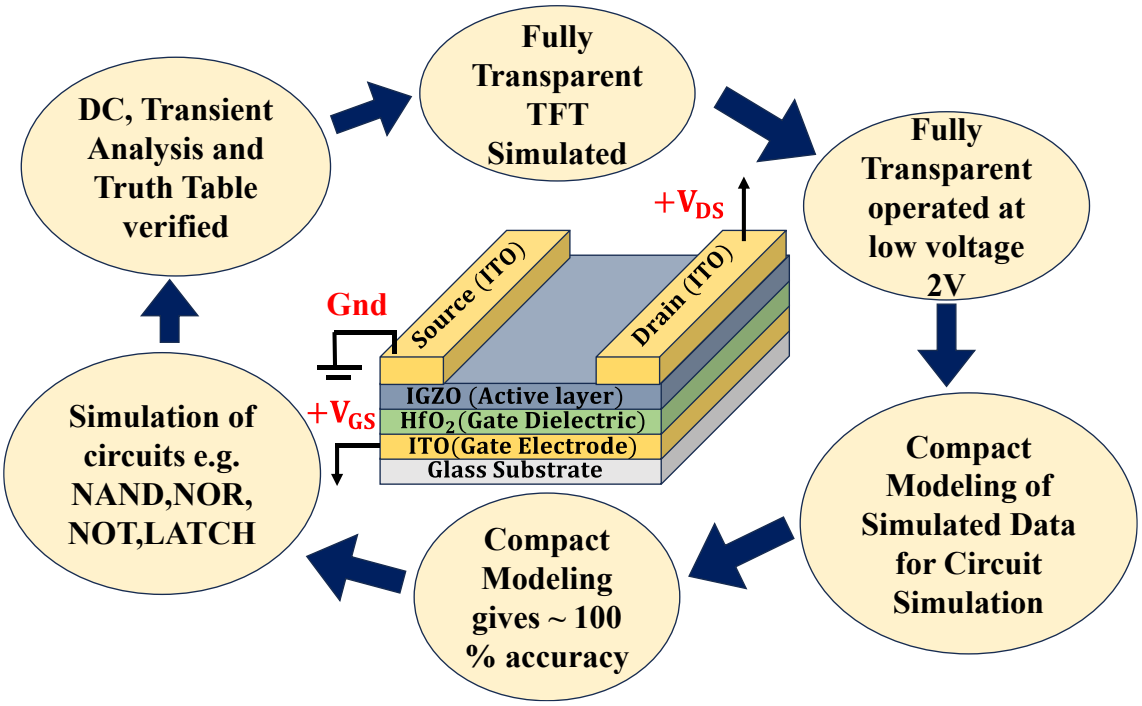


Figure 4.1 Showing the overview of this paper and different steps involved for realizing proposed circuits by this simulated TFT.

Along with the work mentioned above, the Silvaco-Atlas tool a-IGZO-based TFT has been simulated as it is cost- and time-efficient in nature, as directly proceeding with the device fabrication seems risky and costly, but the obtained performance parameters on simulation are still not good as V_{TH} ~ 2 V, SS ~ 90,93 $^{mV}/_{decade}$,operating voltage of 30V, 20V [207]–[209]. The role of compact modeling of simulated, fabricated devices is very essential and important as it develops circuit prototypes, which would be further used for the implementation of various complex circuits as per user specifications and requirements. A number of physical models reside but possess certain restrictions, such as time constraints, limited operating regions, material properties, device structure, etc

[93], [169], [170]. Hence, in this work, a fully transparent, flexible, and compact modeled TFT has been simulated using the Silvaco-Atlas tool, which possesses properties such as a low operating voltage of 2 V, utilization of high-k, that is, HfO_2, as a gate insulator, compact modeling using the Silvaco-Techmodeler tool, and most crucially, implementation of combination circuits as full adders and subtractors using the Silvaco-Gateway tool.

4.2 Device Structure and Specifications

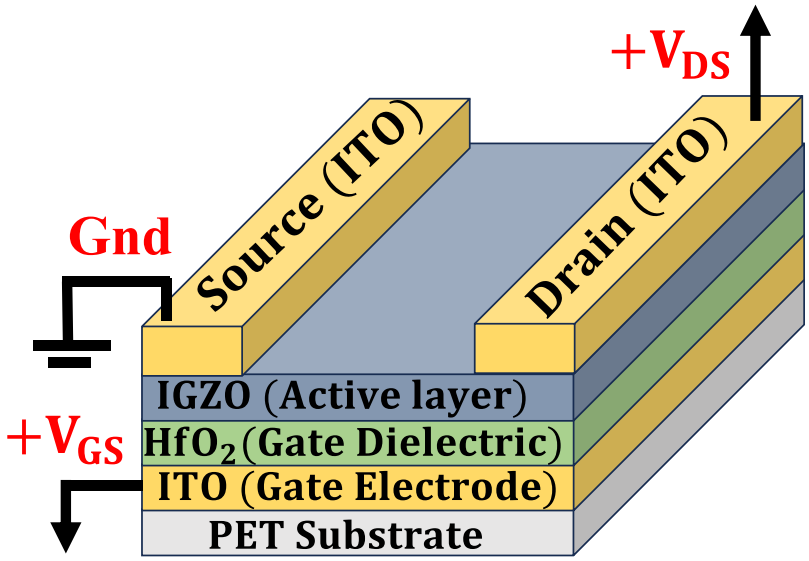


Figure 4.2 Schematic of Fully Transparent TFT when it is subjected to biasing.

Table 4.1 Parameters used for Device Simulation mentioned in this table

Layer Name	Parameter Description	Value	*Ref.
a-IGZO	$N_C\ (cm^{-3})$ Effective DOS in Conduction band	5×10^{18}	[210]
	$N_V\ (cm^{-3})$ Effective DOS in Valence band	5×10^{18}	[210]
	$E_g(eV)$ Band gap	3.25	[184]
	$x\ (eV)$ Electronic Affinity	4.16	[210]
	ε Permittivity	10	[210]
	$\mu_n\ (^{cm^2}/_{Vs})$ Free electron mobility	15	[211]
	$\mu_p\ \left(^{cm^2}/_{Vs}\right)$ Free hole mobility	0.1	[211]
	$T\ (nm)$ Channel Thickness	20	
	$L\ (\mu m)$ Channel Length	30	
	$W\ (\mu m)$ Channel Width	180	
	$N_{TA}(cm^{-3}eV^{-1})$ Density of tail state at $E = E_c$	1.55×10^{20}	[210]
	$N_{TD}(cm^{-3}eV^{-1})$ Density of tail state at $E = E_V$	1.55×10^{20}	[210]
	W_{TA} Conduction band tail slope	0.013	[210]
	W_{TD} Valence band tail slope	0.12	[210]
	$N_{GD}(cm^{-3}eV^{-1})$Donor like Gaussian density state	6.5×10^{16}	[210]
	$W_{GD}\ (eV)$ Characteristics deviation of Donor like Gaussian density state	0.1	[210]
	$E_{GD}(eV)$ The energy peak for the shallow donor-like states	2.9	[210]
HfO_2	$E_g(eV)$ Band gap	4.75	[212]
	ε_{OX} Permittivity	28.5	[212]
	$T\ (nm)$ Dielectric Thickness	60.0	
Source, Drain and Gate Electrode (ITO)	$\varphi(eV)$ Work Function	4.4	[213]
PET Substrate	$T\ (\mu m)$ Substrate Thickness	5.0	

All the parameters required for device simulation and their corresponding details related to all the layers of TFT are specified in **Table 4.1**

In this work, the bottom-gate top contact thin-film transistor (BGTC-TFT) structure is chosen for the evaluation of all the performance parameters, as shown in **Figure 4.2.** For this BGTC-TFT, a-IGZO (amorphous-indium gallium zinc oxide) of thickness 20 nm is used as an active layer; for the gate insulator, HfO_2 is employed with a thickness of 60 nm; and indium tin oxide (ITO) is used as a gate electrode of thickness 40 nm. These layers are deposited over a flexible PET substrate, which is flexible in nature. For the electrodes of the source and drain, the same indium tin oxide (ITO) is utilized for producing this a-IGZO-based fully transparent TFT.

4.3 Silvaco-Techmodeler based Compact Modeling Approach

The TCAD (Technology computer-aided design) based compact modeling approach using the Silvaco-Techmodeler tool is based on a behavior modeling technique in which mathematical and physical specifications are provided by the user. The advantage of this approach is that it reduces the user complexity because large numbers of parameters are interrelated with each other in complex order. In behavior modeling, physical phenomena are modeled using mathematical perception. These models are also referred to as black-box models, as they are not easily managed by manual analysis and exercise. This model is completely based on mathematical formulae, which helps to observe entire physical phenomena in an easier and more simplified way [174].The stages involved in compact modeling of device through Silvaco-Techmodeler tool is shown in **Figure 4.3.**

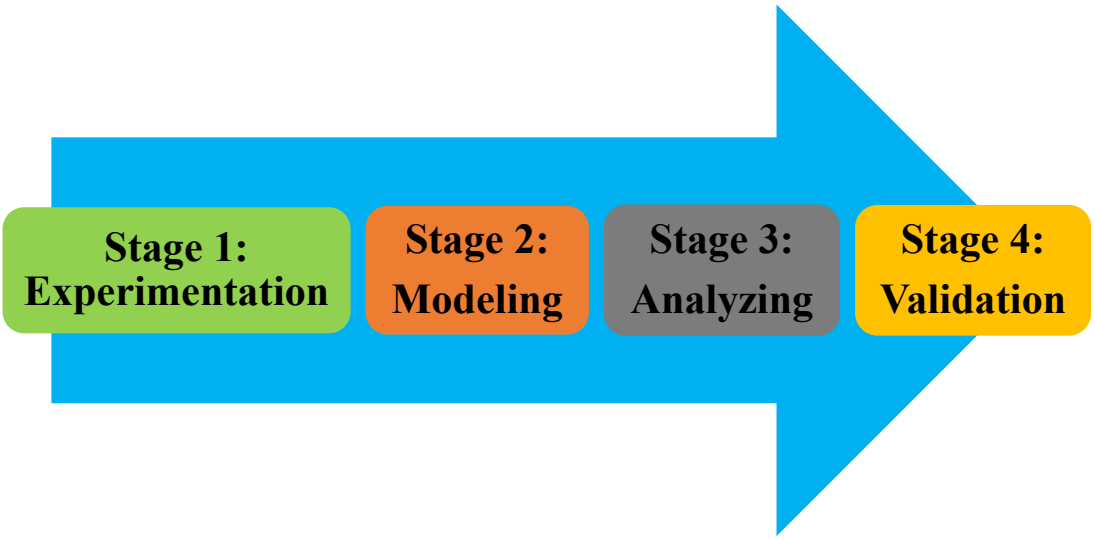


Figure 4.3 Showing the flow of TCAD device modeling process in different stages.

Stages involved in behavior modeling flow are explained as follows:

1. **Experimentation:** In this step, the results of simulations and experiments are provided to the tool. In **Figure 4.4.** The obtained device characteristics are given to the tool.

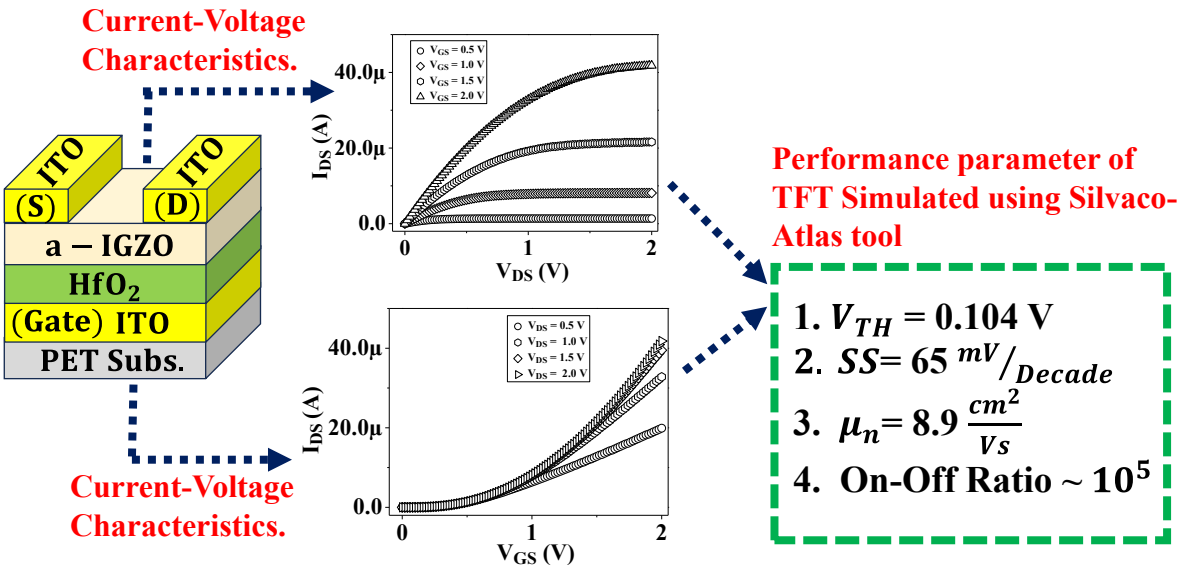
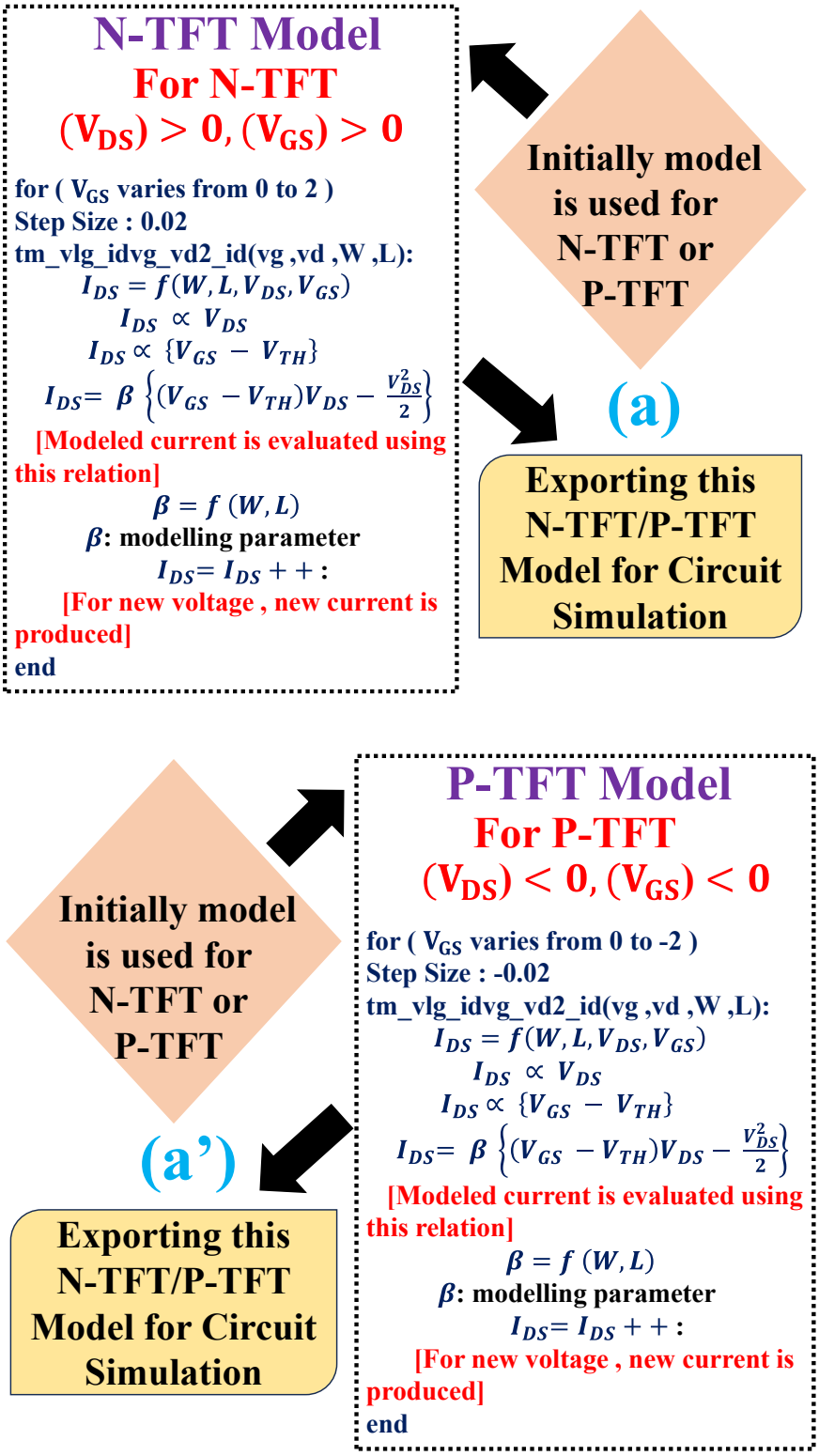


Figure 4.4 Showing the device characteristics data-points which is supplied to Silvaco-Techmodeler tool.

2. **Modeling:** In this step, according to the opted model (N-TFT or P-TFT), corresponding equations are used for the simulation of modeling data, which is expressed in **Figure 4.5.**



Initially, all the device specifications such as width (W), length (L), V_{DS}, V_{GS}, drain current (I_{DS}) of transfer characteristics obtained using simulation / fabrication are provided to Silvaco-Techmodeler tool.

(b)

```
% File../idvg_igzovd2.dat
% Column names: VG ID VD W L
% Name: idvg_igzovd2
% Rows: 101
% Columns: 5
0.00  4.43E-10  2  180E-6  30E-6
0.02  8.89E-10  2  180E-6  30E-6
0.04  1.79E-09  2  180E-6  30E-6
0.06  3.45E-09  2  180E-6  30E-6
.....  .........  .....  .....  .......
.....  .........  .....  .....  .......
```

This algorithm plots the transfer curve (I_{DS} - V_{GS}) from the data points provided by user and through this transfer curve ($I_{DS}^{0.5}$ - V_{DS}) is plotted for the estimation of the threshold voltage (V_{TH}).

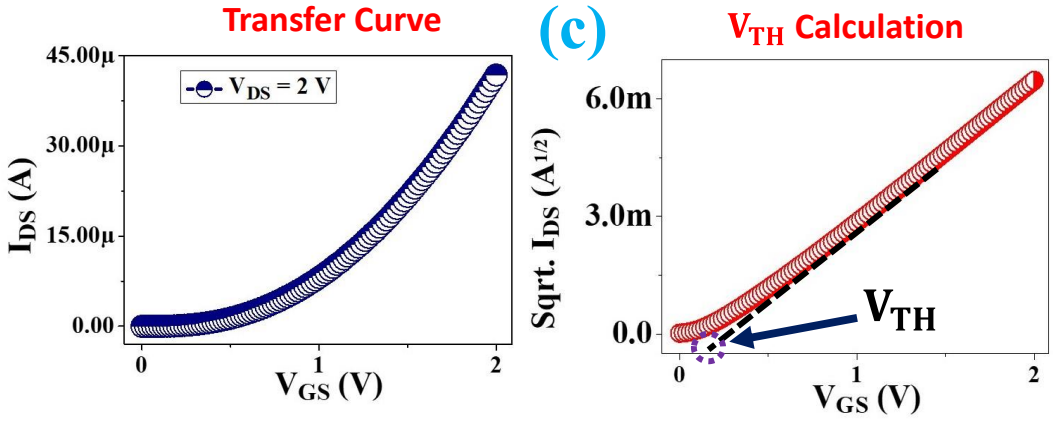
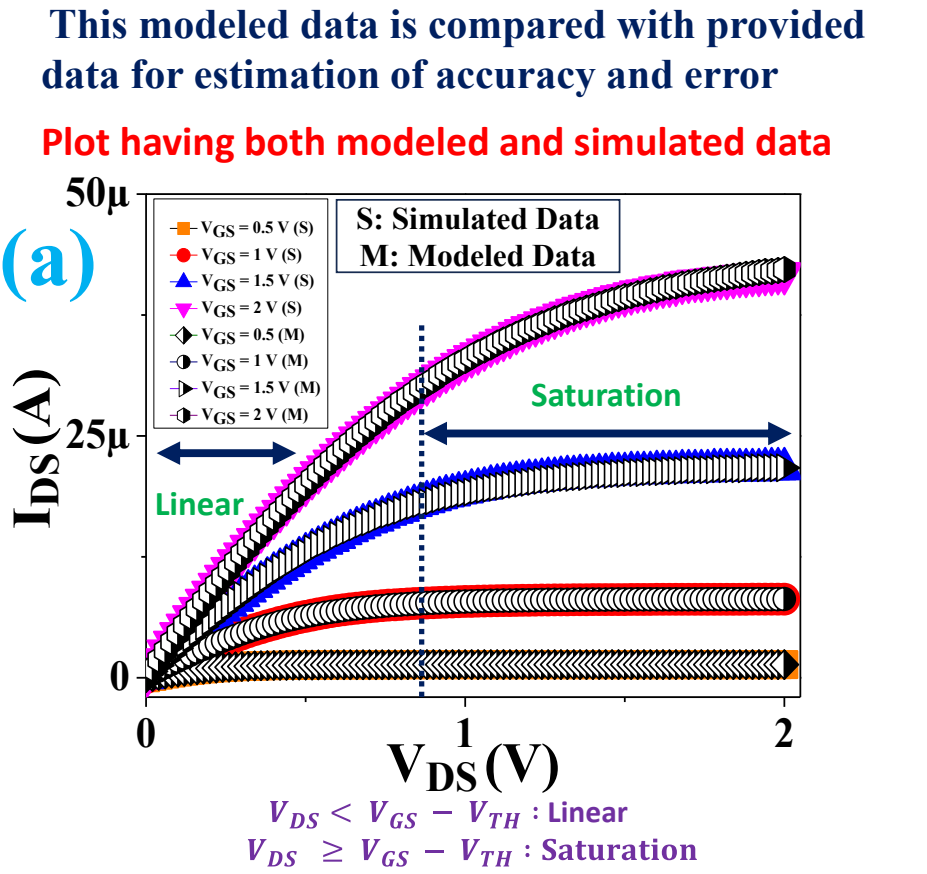
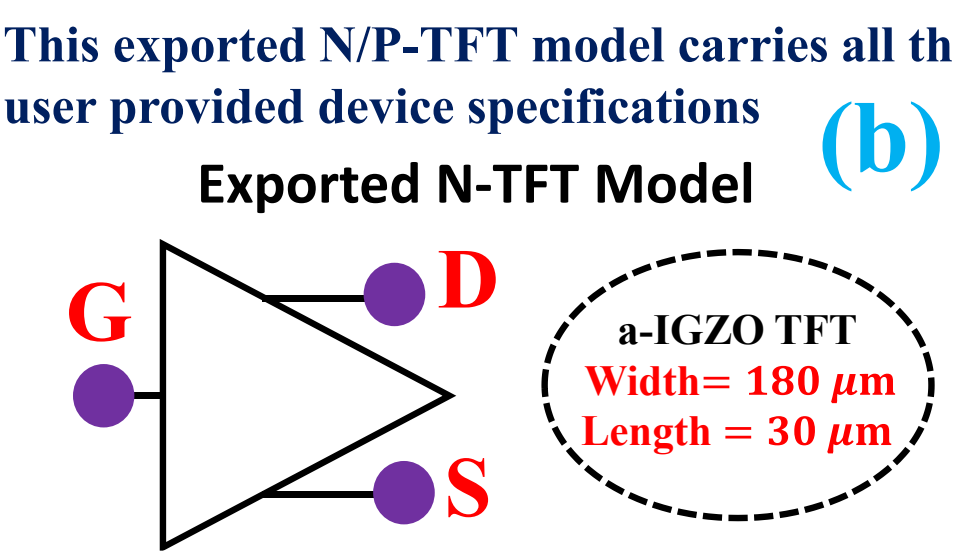


Figure 4.5 (a),(a') (b) and (c) Showing the steps involved in Modeling Stage.

3. **Analysis:** In this section, analysis is performed by estimating the percentage of error versus the supplied data points. Furthermore, errors are estimated between modeled and experimental or simulated data. Exported model can be used for

further analysis. In **Figure. 4.6.** The details associated with analysis stage is shown.





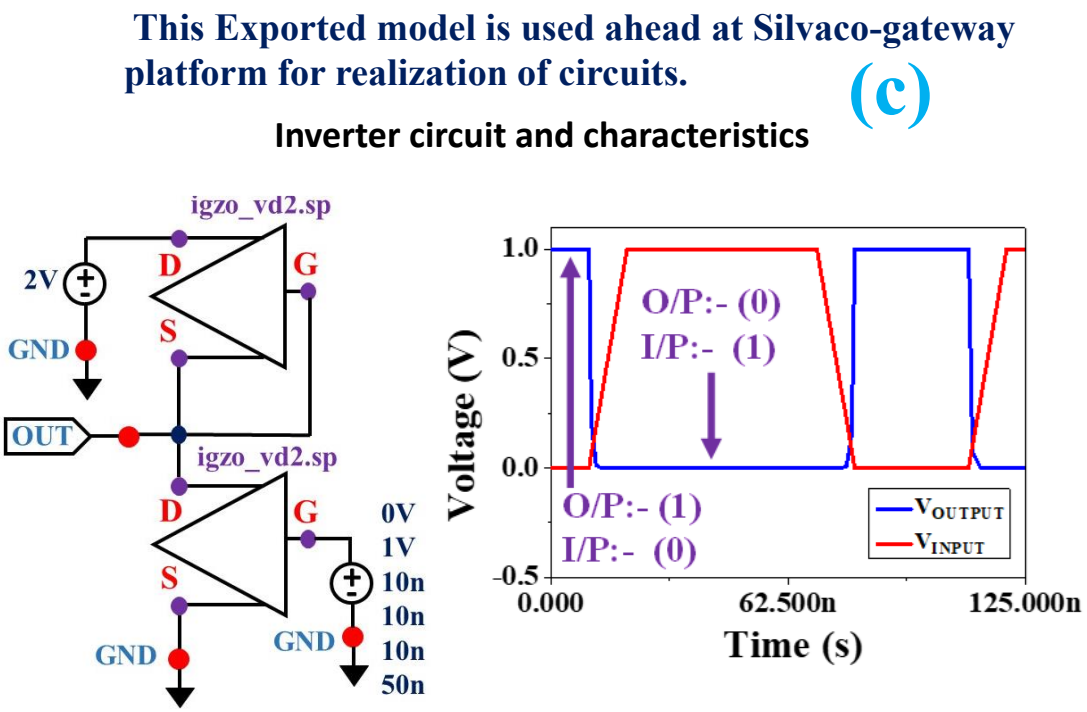
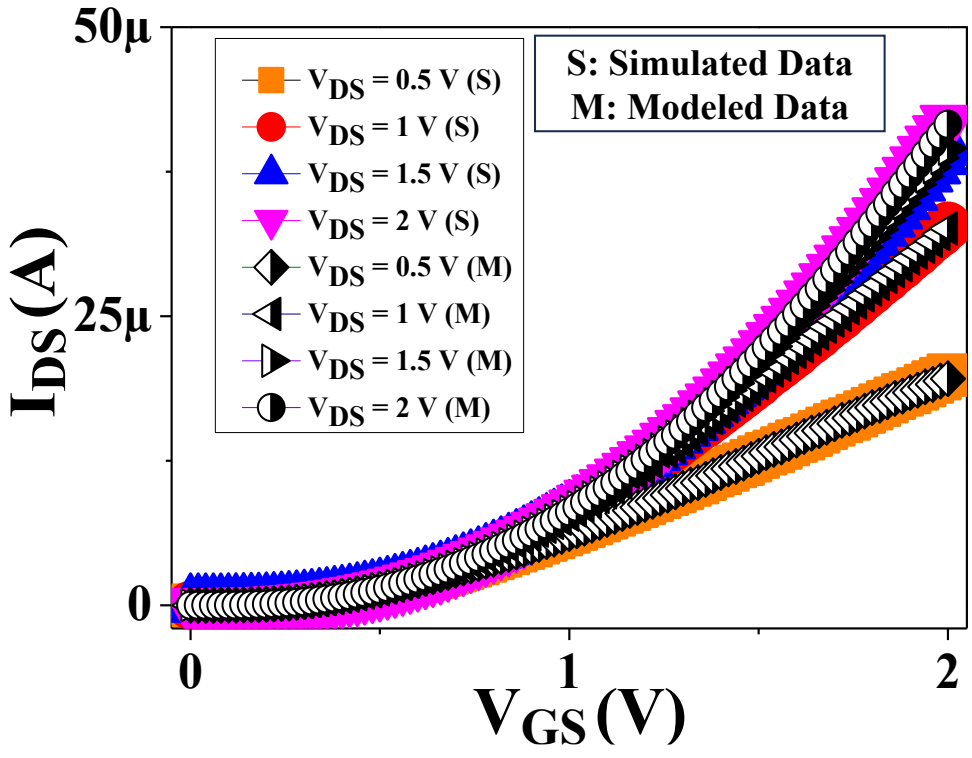


Figure 4.6 (a), (b) and (c) Showing the steps involved in Analysis Stage.

4. **Validation:** Both modeled and experimental/simulated data are verified by the superimposition of both curves on each other shown in **Figure 4.7.**



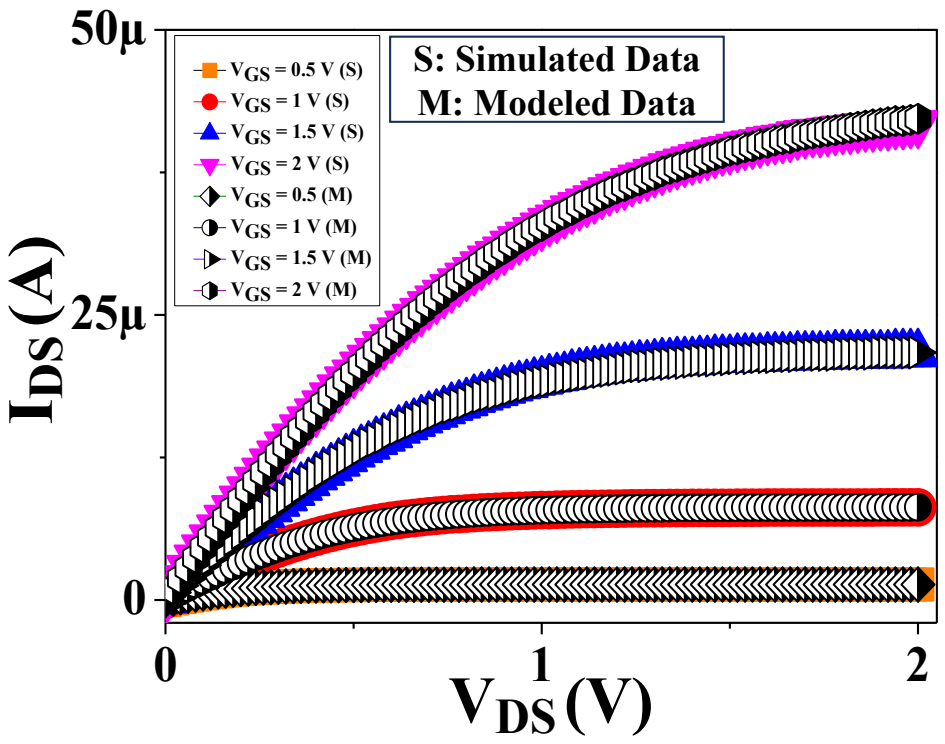


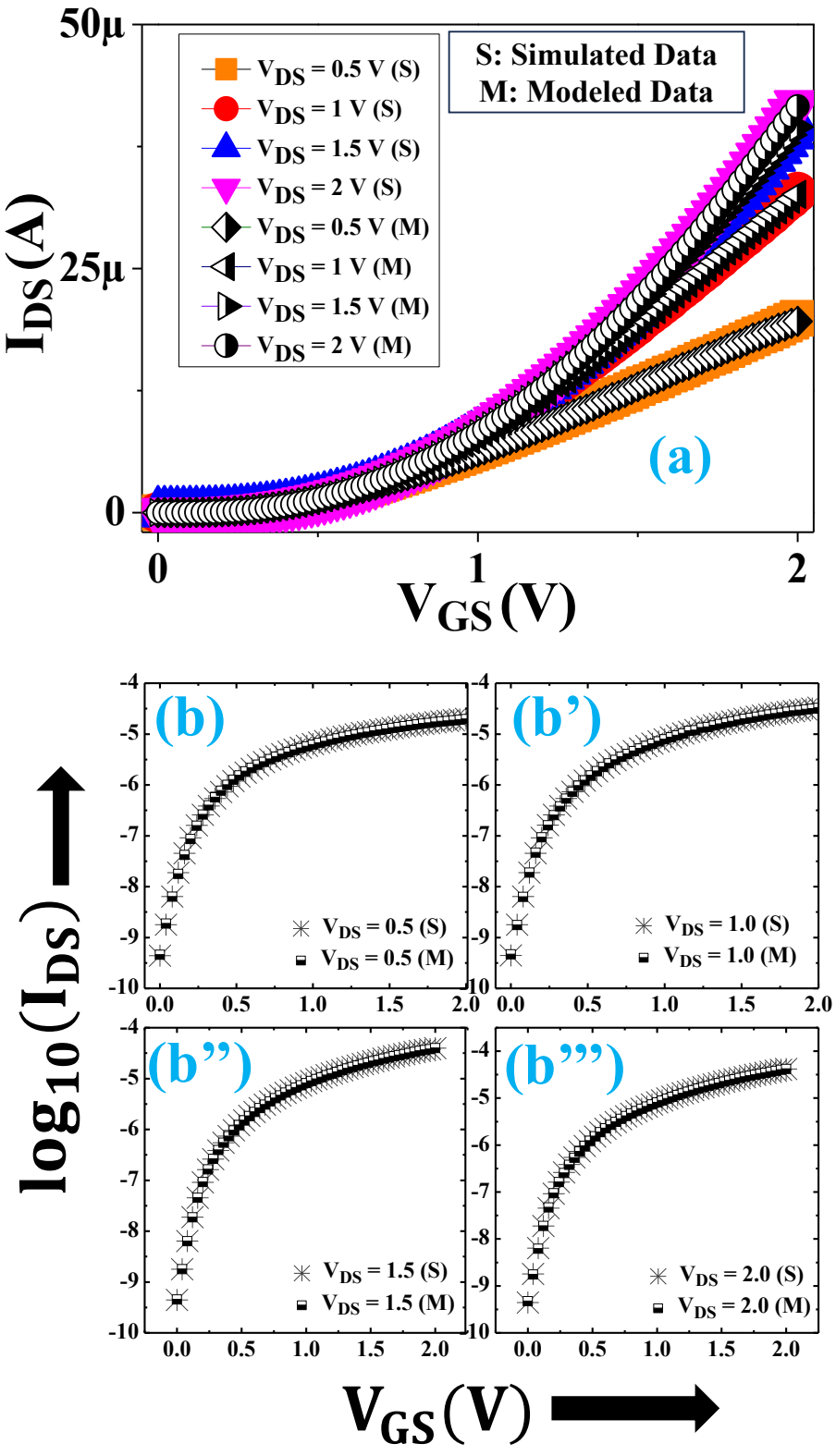
Figure 4.7 Showing the mapping of simulated and modeled data validated small fraction of error between them.

After the validation stage, the performance report is exported, in which all the data points of the experimental, simulated, and modeled curves exist. Along with this, smart-spice files (.sp) and verilog files (.va) can also be exported that contain all the user specifications, i.e., in this case, operating voltage, width, length of device, etc. These (. sp) and (.va) files are further used at the Silvaco-Gateway tool for the realization of circuits.

4.4 Results and Discussions

The Transfer and Output Characteristics are mentioned in **Figure 4.8 (a-d)** which confirm that operating voltage of this device is 2V and saturated current is obtained as 41.8 µA at V_{GS} = 2 V. Silvaco-Techmodeler tool plays a crucial role in compact modeling of the

simulated device, where current voltage data points achieved on device simulation are supplied on this platform and according to these data points (number of iterations) equivalent % error is calculated for both transfer and output characteristics [174].



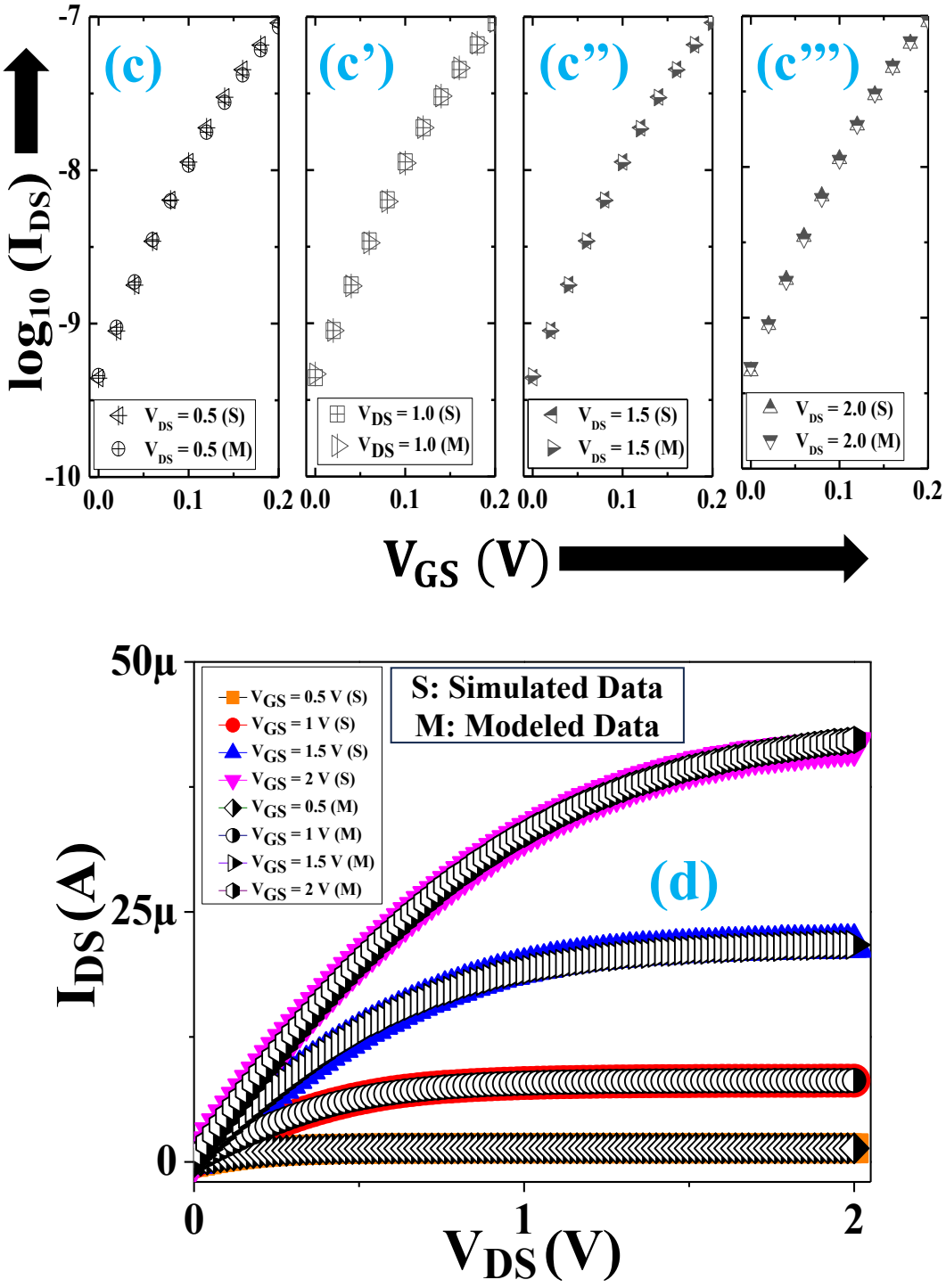


Figure 4.8 (a) Showing the Transfer Characteristics (I_{DS} versus V_{GS} on linear-scale) for V_{DS} varies from 0 to 2 V with an increment of 0.5 V (b-b''') Showing $\log(I_{DS})$ versus (V_{GS}) for V_{DS} varies from 0 to 2 V with an increment of 0.5 V (c-c''') Showing subthreshold region varies from 0 to 2 V with an increment of 0.5 V (d) Showing Output

Characteristics (I_{DS}) versus (V_{DS}) for V_{GS} varies from 0 to 2 V with an increment of 0.5 V.

Figure 4.8 (a) and **(d)** states excellent mapping between simulated and modeled data and few error is observed as 0.41% and 0.94% respectively.

The device operates in two regions:

1. Linear region
2. Saturation region

In linear region, the drain current equation is as follows:

$$I_{DS} = \mu_n C_{OX} \frac{W}{L}\left\{(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right\} \qquad (4.1)$$

For the evaluation of performance parameters, the device should operate in a saturation region whose condition is as follows:

$$V_{DS} \geq V_{GS} - V_{TH} \qquad (4.2)$$

The drain current for the saturation region becomes:

$$I_{DS} = \mu_n \frac{W}{2L} C_{OX}(V_{GS} - V_{TH})^2 \qquad (4.3)$$

$$SS = \left(\frac{d \log I_{DS}}{dV_{GS}}\right)^{-1} \qquad (4.4)$$

Where μ_n is electron-mobility, C_{OX} is oxide capacitance, and W are width and L length of the device. V_{DS} is drain-source voltage, V_{GS} is gate-source voltage, and V_{TH} is threshold voltage. The width (W) and length (L) of this device are taken as 180 μm and 30 μm . The performance parameters of the simulated device are evaluated as $I_{ON}/I_{OFF} \sim 10^5$, $\mu_n \sim 8.9\ {cm^2}/{V_S}$, V_{TH} = 0.104 V and $SS = 65\ {mV}/{decade}$.

With the help of Silvaco-Atlas software, a simulation of the TFT device can be executed for disordered materials and structural specifications.According to the disordered level, inside the semiconductor bandgap defect states vary according to the

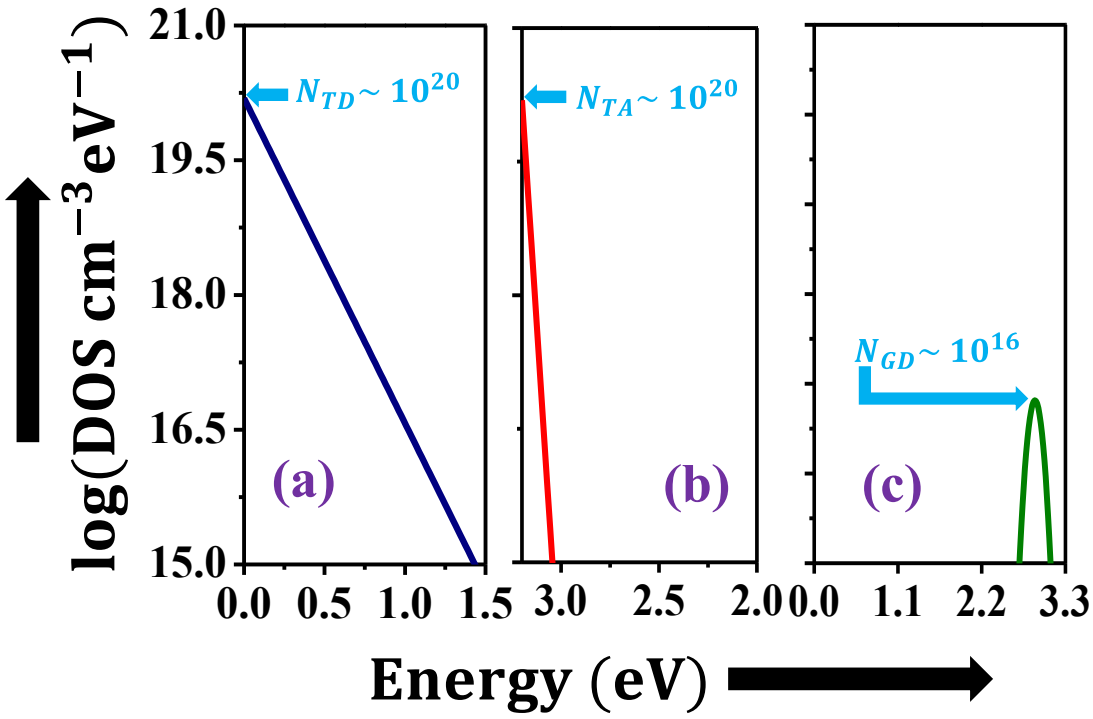
energy allocation, and its associated models are supplied to Atlas. These defect states are referred to as the density of states (DOS), which plays a crucial role in estimating the performance parameters of TFT. These DOS are defined as band-tail states and gaussian distributions [34]–[36].

$$g_{TA}(E) = N_{TA}\, exp\left[\frac{E-E_C}{W_{TA}}\right] \qquad (4.5)$$

$$g_{TD}(E) = N_{TD}\, exp\left[\frac{E_V-E}{W_{TD}}\right] \qquad (4.6)$$

$$g_{GD}(E) = N_{GD}\, exp\left\{-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right\} \qquad (4.7)$$

Where $g_{TA}(E)$, $g_{TD}(E)$ and $g_{GD}(E)$ are defined as acceptor like conduction band tail state, donor like valence band tail, and shallow donor-like gaussian band state, their respective equations are stated above from 4.5 to 4.7. N_{TA} , N_{TD}, N_{GD}, W_{TA}, W_{TD} and W_{GD} are all explained in **Table 4.1.**



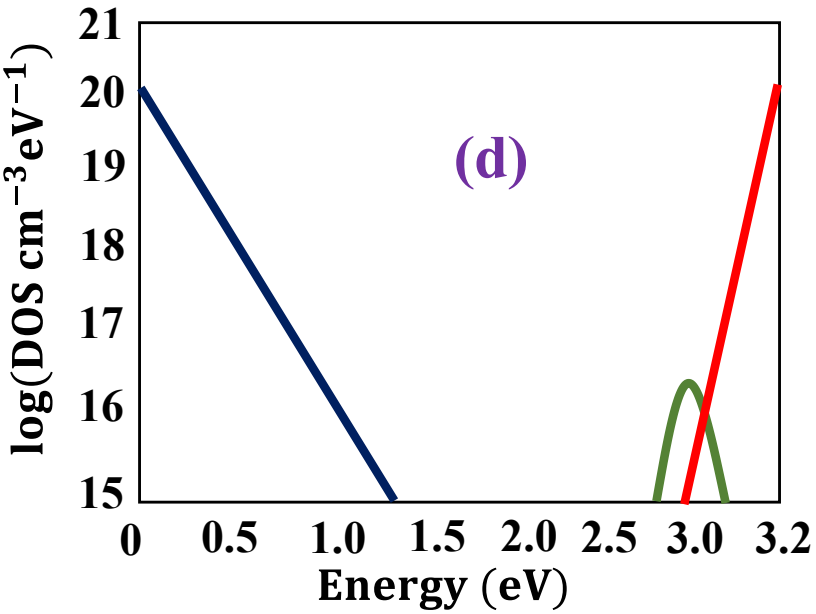


Figure 4.9 (a) Showing log scale of donor like valence band tail state ($g_{TD}(E)$) versus energy curve (b) Showing log scale of acceptor like conduction band tail state ($g_{TA}(E)$) versus energy curve (c) Showing log scale of shallow donor-like gaussian band state ($g_{GD}(E)$) versus energy curve (d) Showing the combined DOS versus energy plots as mentioned in the above parts of Figure 4.9 (a-c).

In the previous reported work, DOS was evaluated, but the plot mentioned in [30] is not just explaining the concentration of DOS (($g_{TD}(E)$), ($g_{TA}(E)$), ($g_{GD}(E)$)) as well as the corresponding energy intercepts where these exist on the energy axis. Similarly, DOS is evaluated and mentioned in [217], but magnitude of W_{TA} , W_{GD} are not specified is not specified as it is directly related to ($g_{TA}(E)$), ($g_{GD}(E)$). **Table 4.1** in this work lists all the parameters used for the evaluation of DOS, and **Figure 4.9** presents the DOS-related plots. **Figure 4.9 (a–d)** for ease of understanding, in which all the peak values of DOS are mentioned.

4.5 Interlinking of Silvaco-Techmodeler and Silvaco-Gateway tools for the realization of Combinational Circuits

The functioning of the Silvaco-Techmodeler and Silvaco-Gateway tools for the realization of combinational circuits and detailed methodology are described in the below statements.

- **Step 1:** In the initial stage, using the Silvaco-Atlas tool, this a-IGZO-based TFT is simulated and, on characterization, generates current-voltage data points, i.e., ($I_{DS} - V_{GS}$) and ($I_{DS} - V_{DS}$).
- **Step 2:** These ($I_{DS} - V_{GS}$), ($I_{DS} - V_{DS}$) readings, operating voltage V_{GS} = V_{DS}= 2 V, width, and length of simulated device as 180 μm, 30 μm . All these values are equipped with the Silvaco-Techmodeler tool.
- **Step 3:** For performing compact modeling, the Silvaco-Techmodeler tool has a modeling section in which the "N-TFT" model is opted for as a-IGZO is n-TFT. In the modeling phase, as per the data points supplied, the corresponding percentage of error is estimated.
- **Step 4:** On 100% execution of this modeling process, modeled data is generated corresponding to the supplied data. This error estimated earlier is reflected here when both modeled data and simulated data are plotted together. The mapping of both modeled data and simulated data for both transfer and output characteristics is shown in **Figure 4.8.** Confirms a small percentage of error is observed (< 1%).
- **Step 5:** This modeled "N-TFT" is imported from the Silvaco-Techmodeler tool in the form of smart-spice (. sp) and verilog (.va) file, which contain all the specifications of the device, such as the operating voltage and device dimension. This imported file, where all specifications are mentioned, is carried out at Silvaco

Gateway Tool, a platform where various complex analog and digital circuits are implemented and further analyzed.

- **Step 6:** In the Silvaco-gateway tool, a pre-existed library remains, which contains a list of basic components like pulse waveform (vpulse), supply voltage (vdd), and ground (gnd). One simulator named Smart-Spice Simulator also exists in this tool, which is used for verifying and obtaining the transient and DC analysis of the respective circuit.

- **Step 7:** Hence Full adder and subtractor circuits are implemented over the Silvaco-Gateway platform with the help of components available in the library, and using the Smart-Spice Simulator, corresponding transient analysis is performed to verify the respective truth tables of the full adder and subtractor.

In Chapter 5, "***Simulation of Digital Circuits Using Compact Modeled N-TFT and P-TFT Devices***", circuitry of Full Adder and Subtractor is shown along with its transient characteristics & respective truth table is mentioned in **"Section 5.9"**.

4.6 Conclusion

In summary, a fully transparent, flexible, and compactly modeled low-voltage TFT has been explored for the implementation of a full adder and subtractor. This simulated a-IGZO-based TFT is compactly modeled using Silvaco-Techmodeler and exhibits excellent accuracy ~ 100%. With the help of Silvaco-Gateway, this compactly modeled TFT works perfectly well in analyzing combinational circuits as full adders and full subtractors, and the corresponding outputs as sum, carry, difference, and borrow are also verified using transient analysis, and the truth table states quite satisfactory results for all possible cases of three inputs. This full adder and subtractor circuit will be utilized in the near future for the execution of complex circuits and memories.

Chapter 5

Simulation of Digital Circuits Using Compact Modeled N-TFT and P-TFT Devices

5.1 Introduction

In past years, the utilization of semiconductor technology in the industrial sectors, such as automobiles, aerospace, etc., and fields such as telecommunications and medicine, are highly impacted by achieving a hike in the development rate. [218]. Such advancement and progress are governed by transistors, which are the fundamental unit of any electronic circuit [219]. Till now, silicon-based transistors have played an important role in chip design. Last six decades for the applications of analog circuits MOSFET's are utilized. There are certain issues associated with MOSFET, such as the Short Channel Effect (SCE), which results in deterioration of mobility, gate leakage current density, an increment in the magnitude of the OFF current, and a small ON current [220]–[224]. Although sometimes Si-based transistors are fabricated using lithography techniques, which are complex in nature [161]. These challenges acted as obstacles to fulfilling today's user needs. In addition to this, thin film transistors and organic thin film transistors (TFT and OTFT)-based devices are highly recognized by the researchers and captured their attention due to their wide range of applications as flexible, wearable, display, sensors, logic circuits, etc. These properties, such as flexibility and transparency, are exhibited by OTFT when PET, polyethylene terephthalate (PET), polyethylene naphthalate (PEN), etc. substrates are employed for fabrication. Similarly, for the fabrication spin coating, floating film transfer (FTM) is one of the methods that is solution-processed and cost-effective in nature. These features have increased the inclination towards OTFT devices [59], [104], [225]–[228]. The functionality of an OTFT device is highly controlled by the materials employed, which are semiconductor layers

and gate insulators [229], [230]. The value of dielectric (k) results in device operating voltage, and this operating voltage further impacts power consumption. Hence, to resolve the constraint of high power consumption, low-operating voltage (1-2 V) TFT devices are developed in which high-k dielectrics such as ZrO_2 and HfO_2 are used [201], [231]–[235]. Along with this, these dielectrics help to overcome the issue of tunneling gate leakage current as faced by MOSFET's where SiO_2 is used as a dielectric [236]. The final objective of a perfectly working simulated or fabricated TFT device is to use it further for IC design. As previously reported, TFTs were fabricated and simulated using the Atlas-Silvaco tool, but they were limited to the evaluation of performance parameters only [131], [224], [237]–[239]. Furthermore, they are not utilized for the implementation of analog and digital circuits. Hence, to realize the circuits from the simulated or fabricated device, compact modeling plays a crucial role as it develops circuit prototypes according to user demand, which helps further circuit implementation. In order to perform the compact modeling, some physical models already existed but upheld obligations such as material properties, a finite region of operation, and device specifications [93], [169], [170]. Hence, to overcome these challenges, the TCAD-based compact modeling technique is opted for due to the reduction in complexity users suffer while dealing with parameters that are linked with each other in a complex way [174]. In this work, a user guide is developed, and all the steps are mentioned for compact modeling of the device achieved either by simulation or fabrication with the help of the Silvaco-Techmodeler tool. Also, using this compact modeled device, any type of analog or digital circuit can be implemented using the Silvaco-Gateway tool. This Silvaco-Gateway tool contains a smart-spice simulator that is used to analyze the DC and transient behavior of the desired circuit for the estimation of parameters such as noise margin, propagation delay, gains, etc [101]. Using the steps mentioned in the below sections, a low-voltage flexible TFT's

have been compact modeled for the realization of combinations circuits as Half-Adder, Full Adder and Subtractor, basic logic gate families, 4:1 multiplexer circuit and 1-Bit ALU circuit has also been implemented using these compact modeled devices [94], [96]–[100].

5.2 Steps Involved in Compact Modeling and Circuit Simulation using Silvaco-Techmodeler and Silvaco-Gateway Tools

In the initial step, device specifications such as operating voltage (V_{GS}, V_{DS}), channel length (L), width (W) along with these parameters current-voltage measurements (I_{DS} - V_{GS}), (I_{DS} - V_{GS}) that are obtained using device simulation or fabrication, are provided to the Silvaco-Techmodeler tool. In **Figure 5.1**, a schematic is shown where these parameters and their corresponding order of arrangement are mentioned.

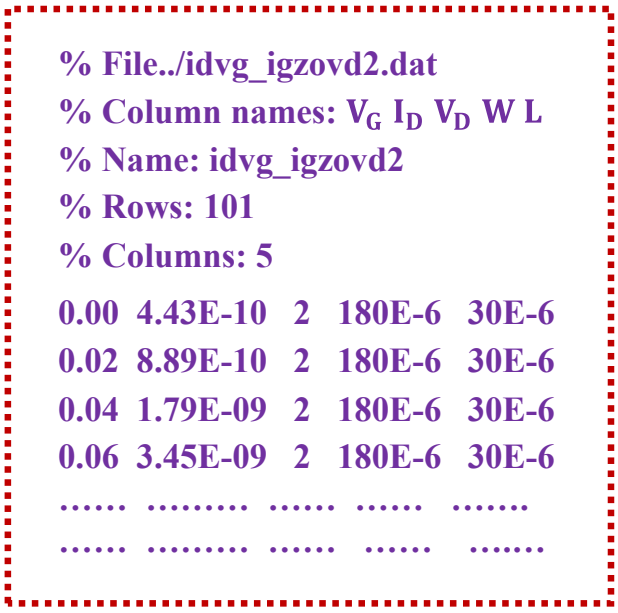


Figure 5.1 Shows template in which device parameters are displayed which would be provided to the Silvaco-Techmodeler tool.

In **Figure 5.2**, all the parameters associated with the devices that are mentioned in the template shown in **Figure 5.1**. are loaded into the Silvaco-Techmodeler tool. In **Figure**

5.1, a total of 5 variables are used in a similar way; 5 model variables are mentioned in the tool along with their corresponding units and orientation. The project name and description were kept the same as the loaded source file name for ease of understanding only. The orientation of I_D is kept as output; the rest all are kept as input, as current values vary according to the change in magnitude of V_G and V_D. All the parameters used in the loaded file are mentioned with their units in **Figure 5.2.**

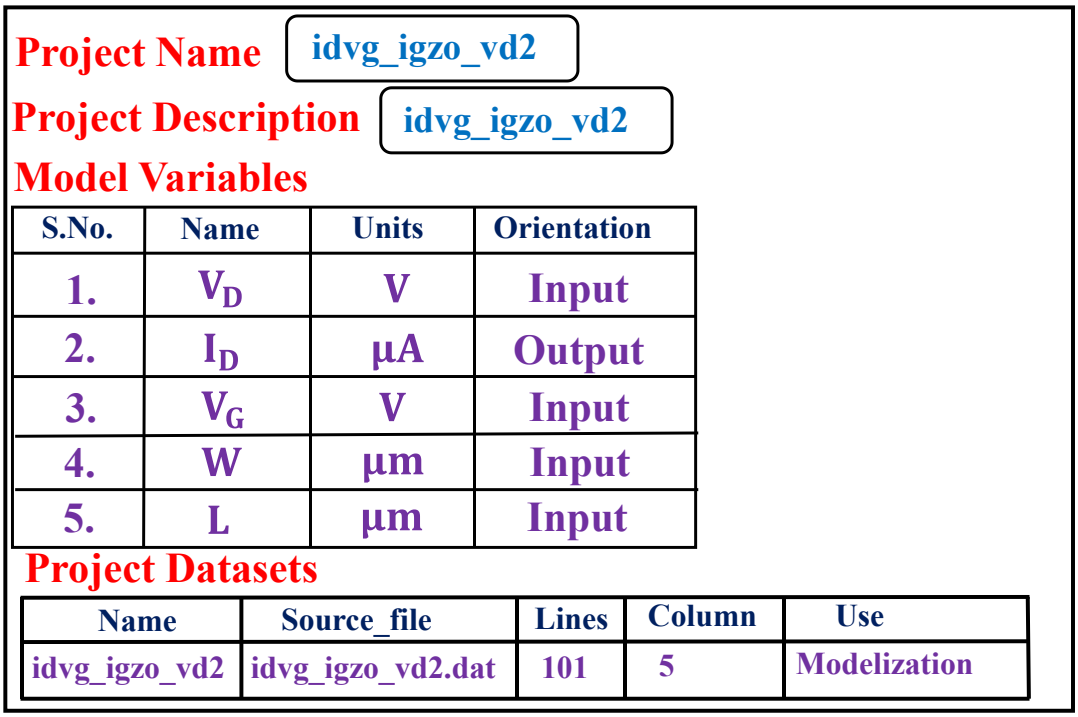


Figure 5.2 Showing the diagram of Silvaco-Techmodeler tool, where device parameters file are loaded to this tool.

In addition to this, according to the device type simulated or fabricated, the same type of model, either P-TFT or N-TFT, is selected, which is displayed in **Figure 5.3**. As the orientation of variable I_D is output, a quadratic error is estimated between experimental or simulated results and modeled results.

Project Name idvg_igzo_vd2

Project Description idvg_igzo_vd2

Model Variables

Model-Type: N-TFT

S.No.	Name	Units	Orientation	Error -Type
1.	V_D	V	Input	-----
2.	I_D	µA	Output	Quadratic
3.	V_G	V	Input	-----
4.	W	µm	Input	-----
5.	L	µm	Input	-----

Figure 5.3 Showing the diagram of Silvaco-Techmodeler tool, where according to the loaded data file and device type, model is selected.

When current-voltage data points are supplied according to which % error is estimated, which is also evaluated and mentioned in **Figure 5.4.**

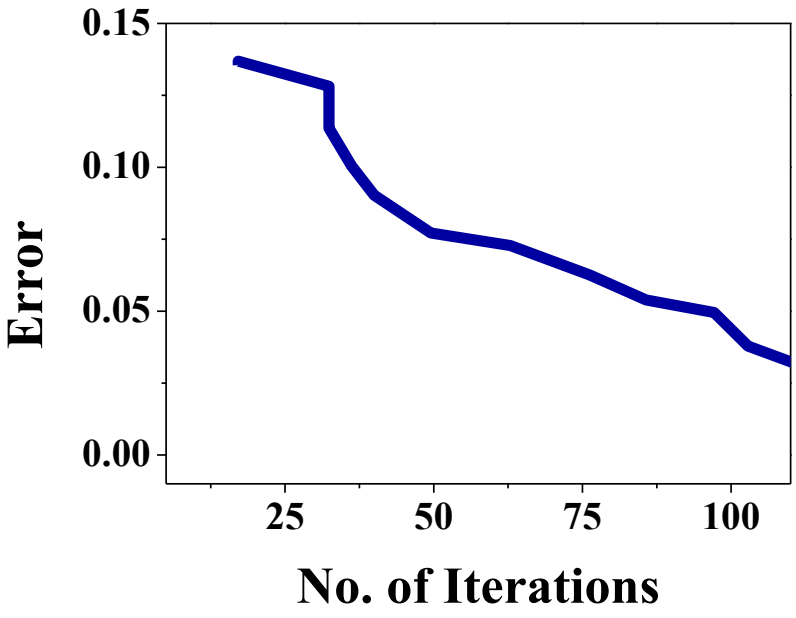


Figure 5.4 Shows the error calculation for all the iterations (data-points) between modeled data and experimental/simulated data.

In the Silvaco-Techmodeler tool, modeler section, different options are available as variables, data, models, etc., as shown in **Figures. 5.5 to 5.7**.

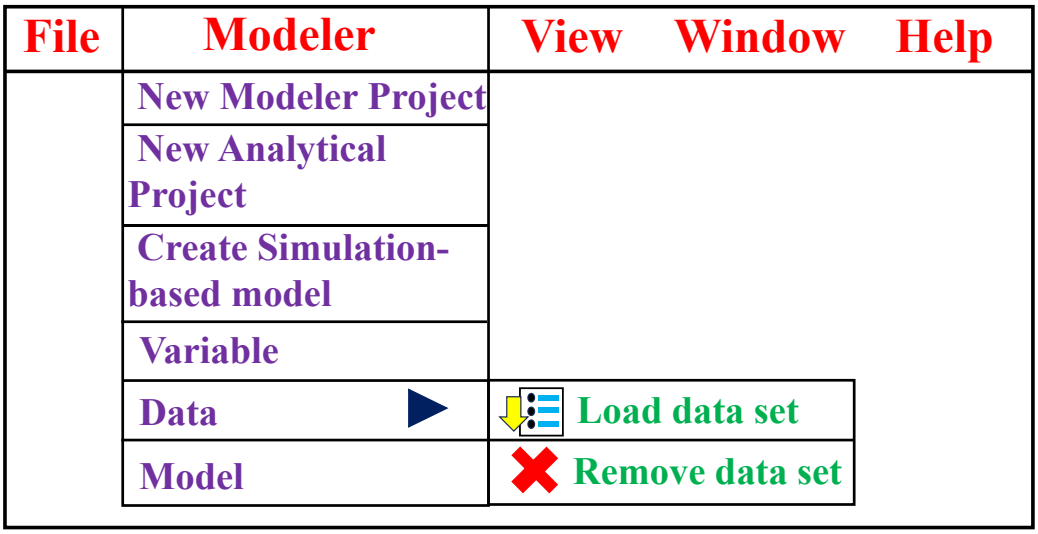


Figure 5.5 Shows the modeler section in which among different options the classification of data option is displayed.

Initially, in the data subsection of the modeler part shown in **Figure 5.5**, the data files are loaded, which contain all the device specifications. The device parameters are arranged in a similar manner as displayed in the template in **Figure 5.1**. If, by mistake, any different file is uploaded by the user, then another option also exists to remove the data file so that file can be easily eliminated. Other issues may result, such as errors, etc. In **Figure 5.6**, the variable subsection contains two options: variable creation and deletion. If the user wants to add or remove any further variables in loading the data files, this subsection would be useful for its execution. This model subsection plays a crucial role as it contains options such as model creation, modelization, detailed performance reports, model exportation, etc. In the create model section, according to the nature of the device, a simulated or fabricated model is opted for and further proceeded.In the modeling section,

a process takes place in which, according to the supplied data points, the corresponding error is estimated.

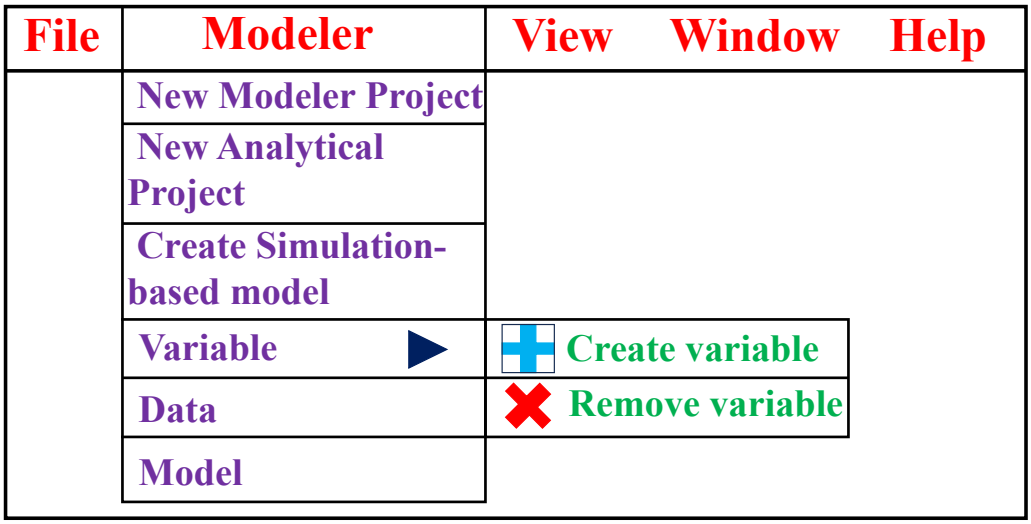


Figure 5.6 Shows the modeler section in which among different options the classification of variable option is displayed.

Along with these two subsections, one more subsection exists that is very crucial and important, named the model subsection shown in **Figure 5.7**.

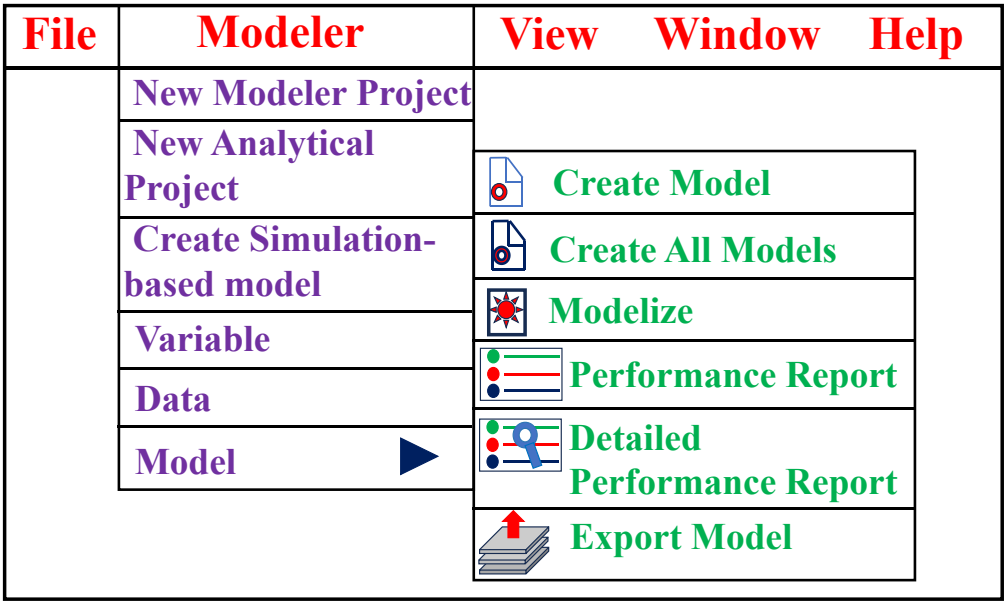


Figure 5.7 Shows the modeler section in which among different options model option is elaborated in classified manner.

This error evaluation with respect to the iteration numbers is shown in **Figure 5.4**. In a detailed performance report, according to the employed data points, modeled data is generated, and the magnitude of error and percentage are calculated between these two sets of data.

Detailed Performance Report

Data Number	I_D (Data)	I_D (Modeled)	Error	% Error
igzo_vd2_1	4.18×10^{-5}	4.16×10^{-5}	1.73×10^{-7}	0.41
igzo_vd2_2	4.09×10^{-5}	4.07×10^{-5}	1.53×10^{-7}	0.37
igzo_vd2_3	4.00×10^{-5}	3.99×10^{-5}	1.29×10^{-7}	0.32
igzo_vd2_4	3.91×10^{-5}	3.90×10^{-5}	1.01×10^{-7}	0.26
igzo_vd2_5	3.82×10^{-5}	3.81×10^{-5}	6.82×10^{-8}	0.18
igzo_vd2_6	3.73×10^{-5}	3.73×10^{-5}	3.04×10^{-8}	0.08
igzo_vd2_7	3.64×10^{-5}	3.64×10^{-5}	1.26×10^{-8}	0.03
igzo_vd2_8	3.55×10^{-5}	3.56×10^{-5}	6.14×10^{-8}	0.17
.....	.....	.....	.....	.....

Figure 5.8 Shows the parameters involved in detailed performance report.

In **Figure 5.8**, all the sections stated above for a detailed performance report are shown. A smaller error is observed between loaded data and modeled data, resulting in excellent mapping between these data. In addition to this, one more option is available, which is the export model, through which the entire model is exported. This exported model contains all specifications that are mentioned in the smart-spice file and the verilog file. In **Figure 5.9**, the details associated with these files are explained. These files (smart-spice and verilog files) are further used at the Silvaco-Gateway tool for the realization of different analog and digital circuits.

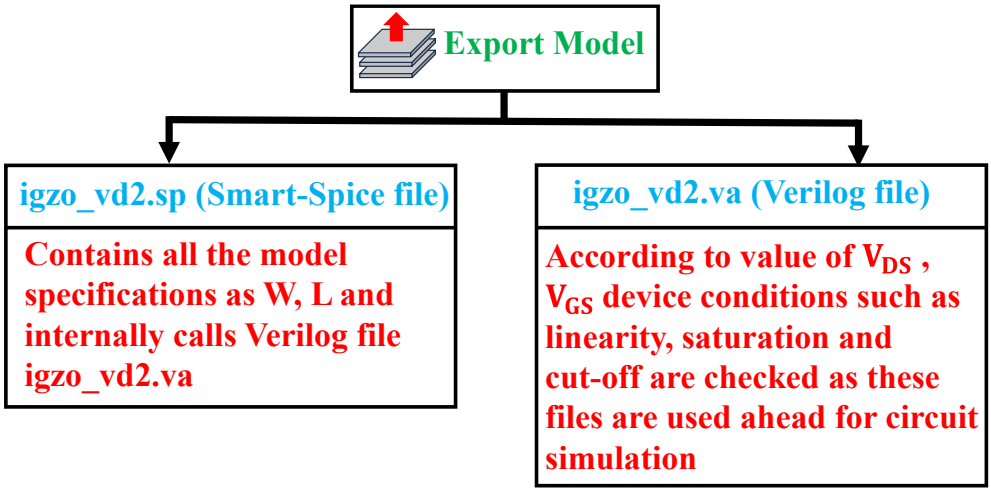


Figure 5.9 Shows the exported model files in detailed manner.

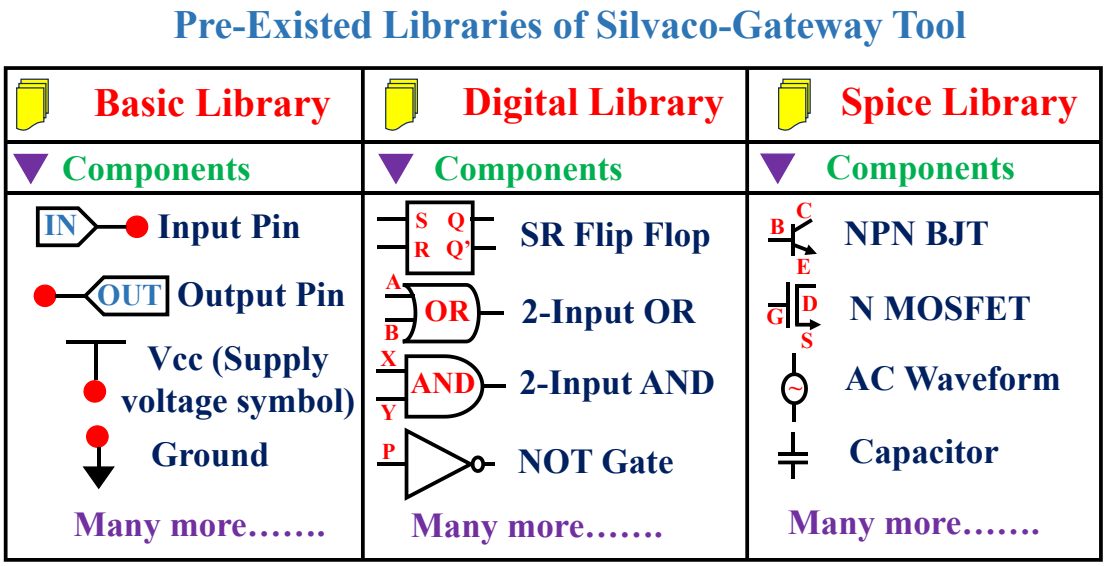


Figure 5.10 Listed all the libraries and it's components with reside in Silvaco-Gateway tool.

In **Figure 5.10**, the list of libraries is shown as basic library, digital library, and spice library. In every library, all the associated components are displayed. These basic components are very important, as with their help, any type of complex circuit can be implemented and realized. In addition to these components, some input and output pins also exist, which are used when both input and output waveforms are to be visualized.

This exported model, as mentioned above in **Figures 5.7 and 5.9**, is imported here at the Silvaco-Gateway tool, as shown in **Figure 5.11**.

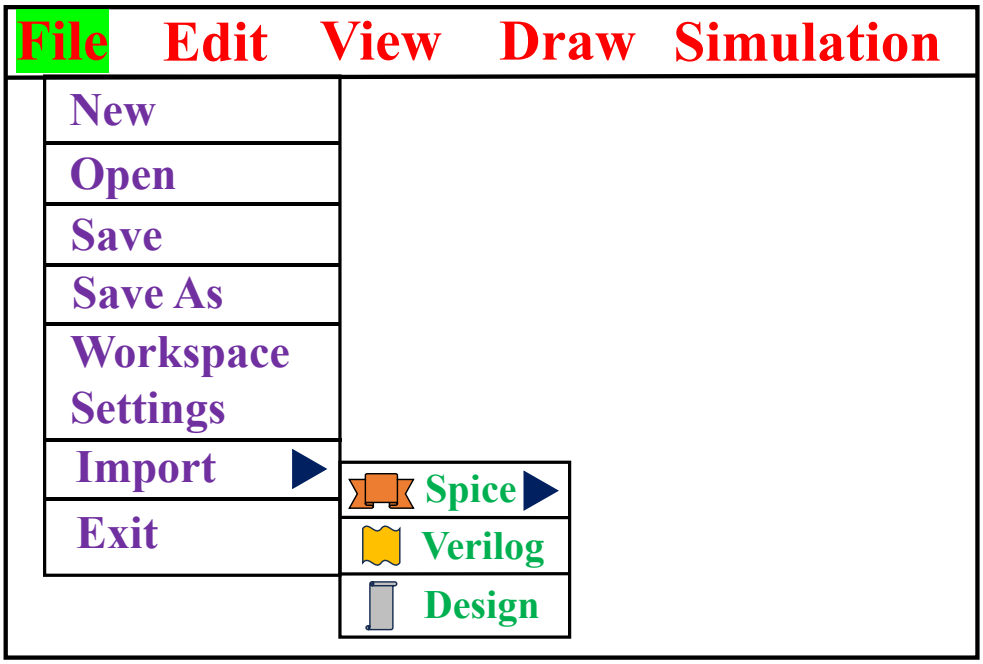


Figure 5.11 Shows the parameters involved in detailed performance report.

In the import section, available options are spice, verilog, etc. Among these options, a smart-spice file, e.g., igzo_vd.sp, is selected. This igzo_vd.sp file holds all the parameters associated with the device stated above, and along with this, it internally calls the verilog file. The reason for calling this verilog file is for the verification of device operations. In **Figure 5.12**, all the steps are mentioned, which state the path, location, and name of this.sp (smart-spice file). In a similar way, a new symbol for this compact-model device is also selected, which contains all three terminals of TFT as source, gate, and drain, as shown in **Figure 5.13**. Along with these terminals, the dimensions of this symbol, such as channel width and length, are the same as previously mentioned.

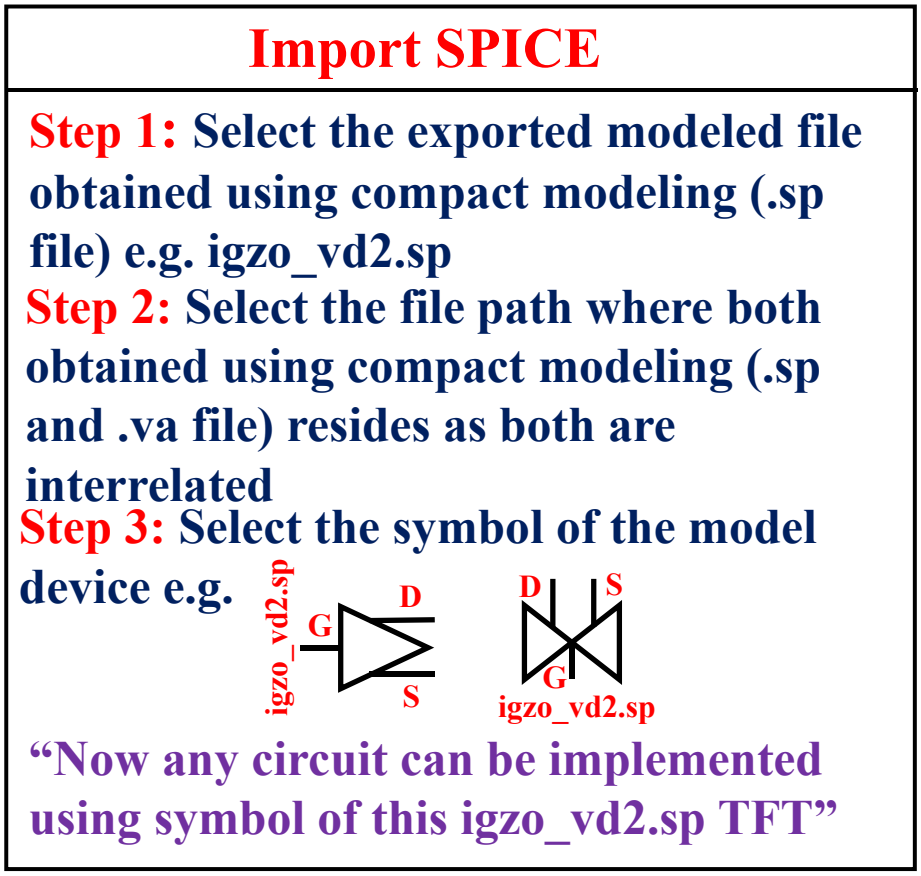


Figure 5.12 Steps involved to import this exported model are mentioned.

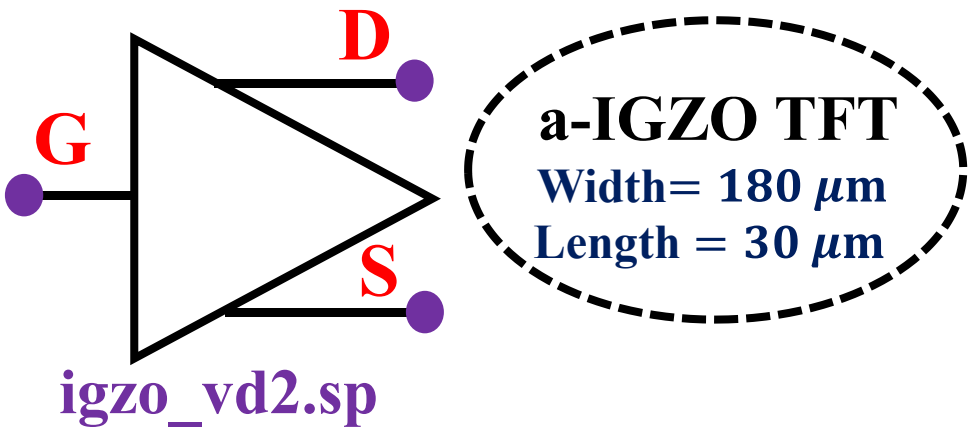


Figure 5.13 Showing the symbol of modeled device and its associated dimensions.

This simulated or fabricated device is compactly modeled using the Silvaco-Techmodeler tool. **Figure 5.8** states the detailed performance report in which both modeled data and loaded data are mentioned.

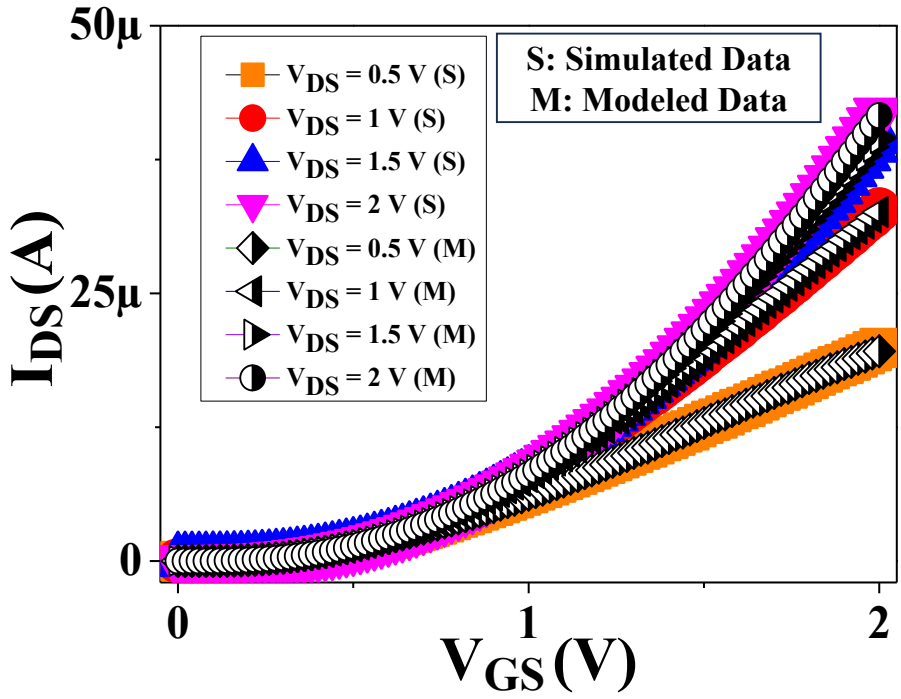


Figure 5.14 Showing the Transfer Characteristics ($I_{DS} - V_{GS}$) for V_{DS} varies from 0 to 2V with a step size of 0.5 V [235].

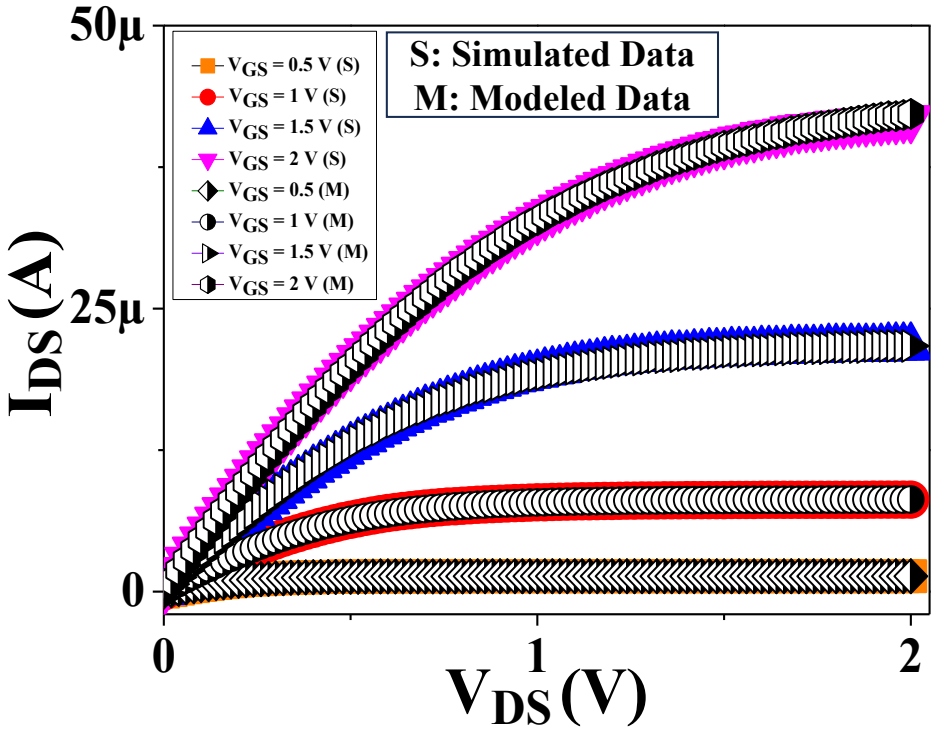


Figure 5.15 Showing the Output Characteristics ($I_{DS} - V_{DS}$) for V_{GS} varies from 0 to 2V with a step size of 0.5 V [235].

In **Figures 5.14 and 5.15,** plots between both simulated and modeled data are displayed, which proclaims perfect mapping and excellent superimposition for these data [235]. The schematic of a thin-film transistor with new device specifications is shown in **Figure 5.13**. Now, using this device, any type of complex circuit can be analysed and implemented using the Silvaco-Gateway tool. For example, using this "igzo_vd2.sp" file, which contains device dimensions such as channel width and length of 180 and 30 is utilized for the realization of an inverter circuit as shown in **Figure 5.16**.

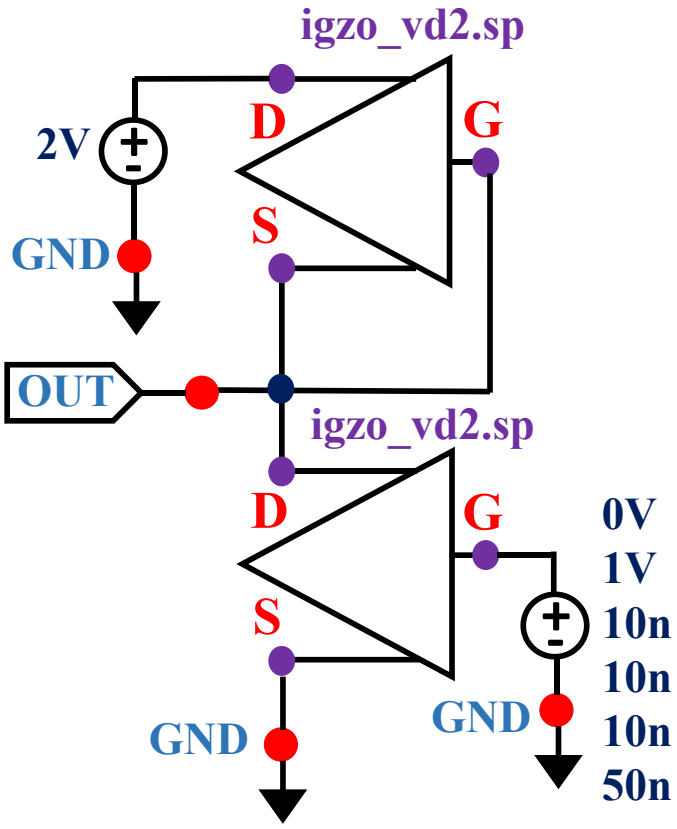


Figure 5.16 Showing the Inverter Circuit implemented using exported "N-TFT".

In order to check the proper working and functionality of this inverter circuit, its corresponding transient analysis and DC analysis are performed, which are shown in **Figures 5.17 and 5.18**. This transient behavior is time-variable, whereas DC analysis is

time-independent. These two analyses help with the evaluation of various parameters as average propagation delay (τ_p) , gain, noise margin (NM_{OV}) etc.

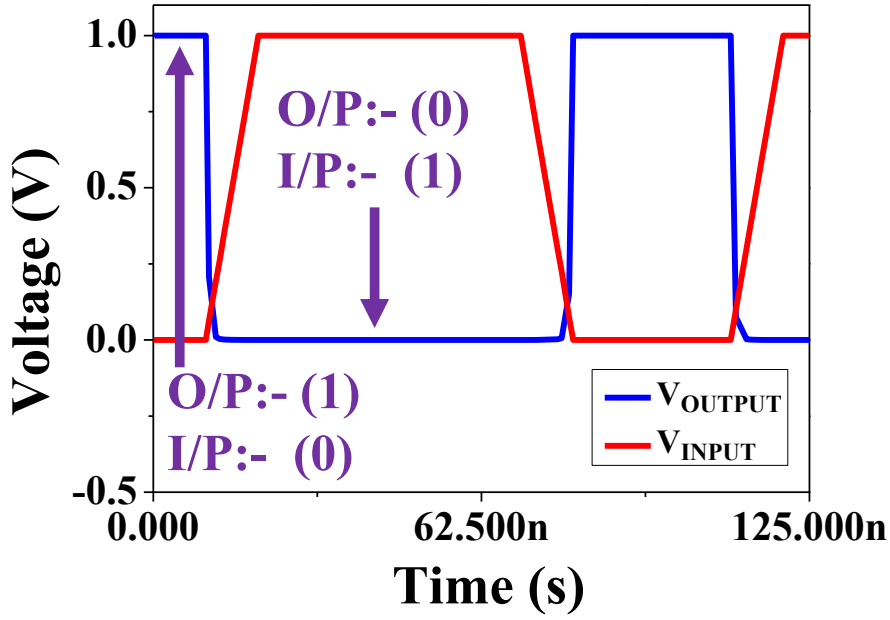


Figure 5.17 Showing the transient behaviour of this implemented inverter circuit.

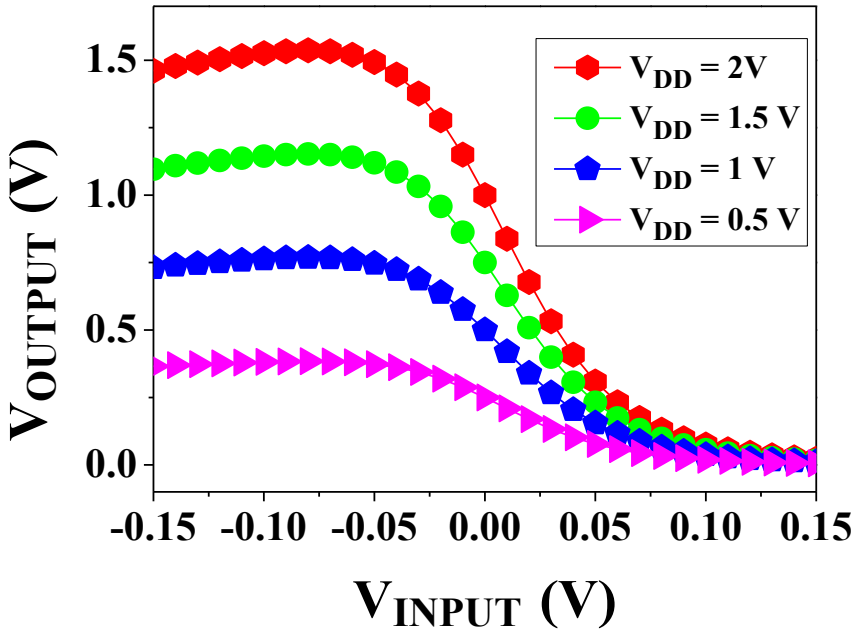
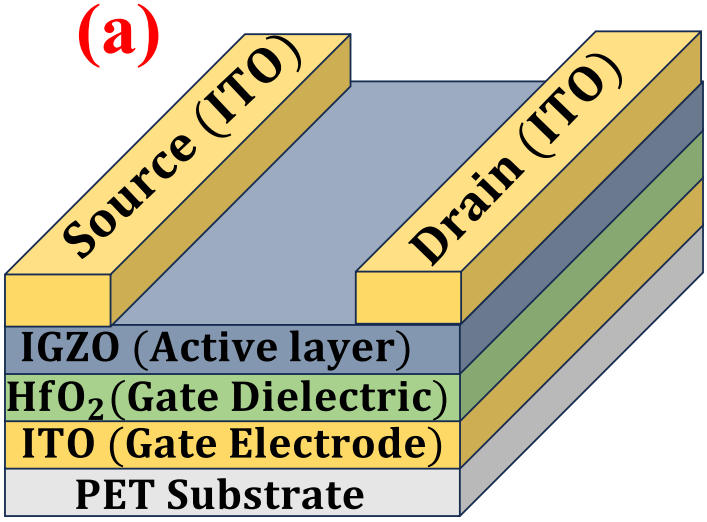


Figure 5.18 Showing the voltage transfer characteristics of this implemented inverter circuit.

5.3 Device Structure and Characteristics

(a)



Device Specification

1. Channel Length ~ 30 μm
2. Channel Width ~ 180 μm
3. Channel Thickness ~ 40 nm
4. Dielectric Thickness ~ 60 nm
5. Source, Drain Contact : ITO
6. Gate Electrode : ITO
7. Active Layer: IGZO
8. Gate Dielectric: HfO_2

IGZO : Indium gallium zinc oxide

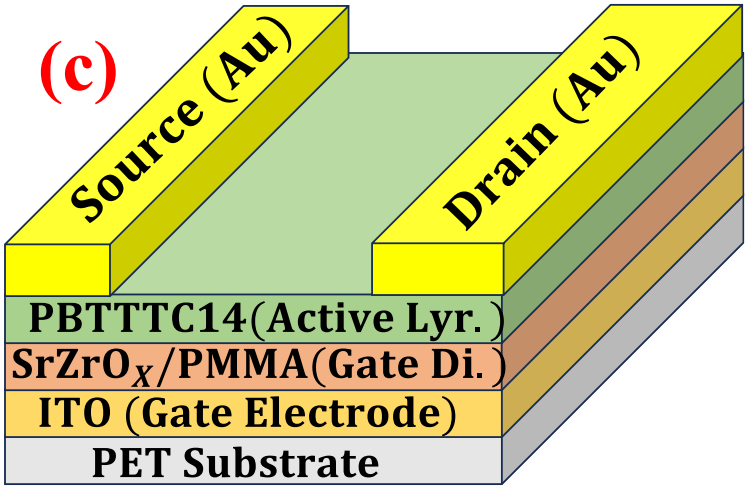
ITO : Indium Tin oxide

(b)

Performance Parameters

1. V_{TH} = 0.1 V
2. $SS = 65\ {}^{mV}/_{Decade}$
3. $\mu_n = 8.99\ \frac{cm^2}{Vs}$
4. On-Off Ratio ~ 10^5

(c)



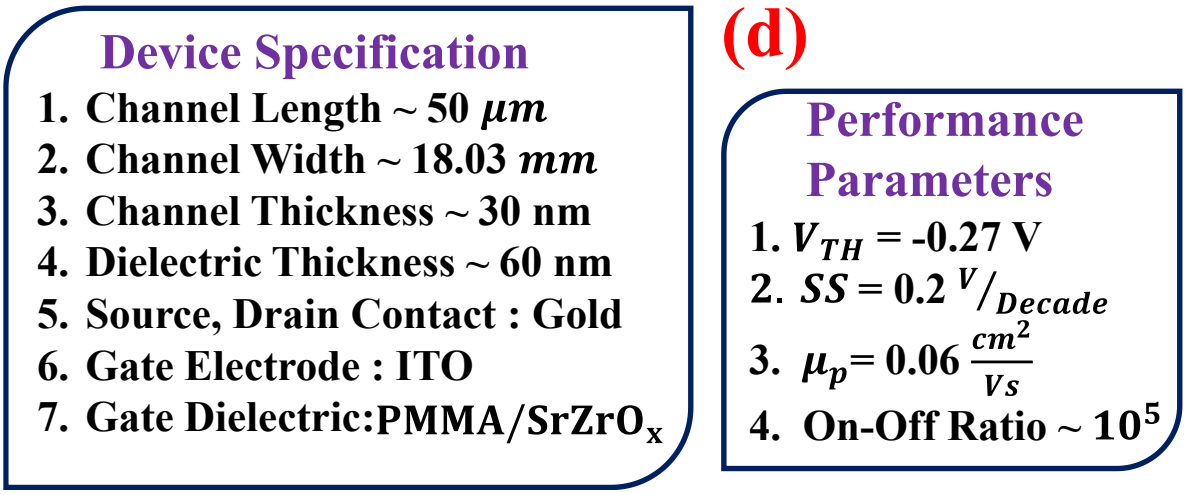
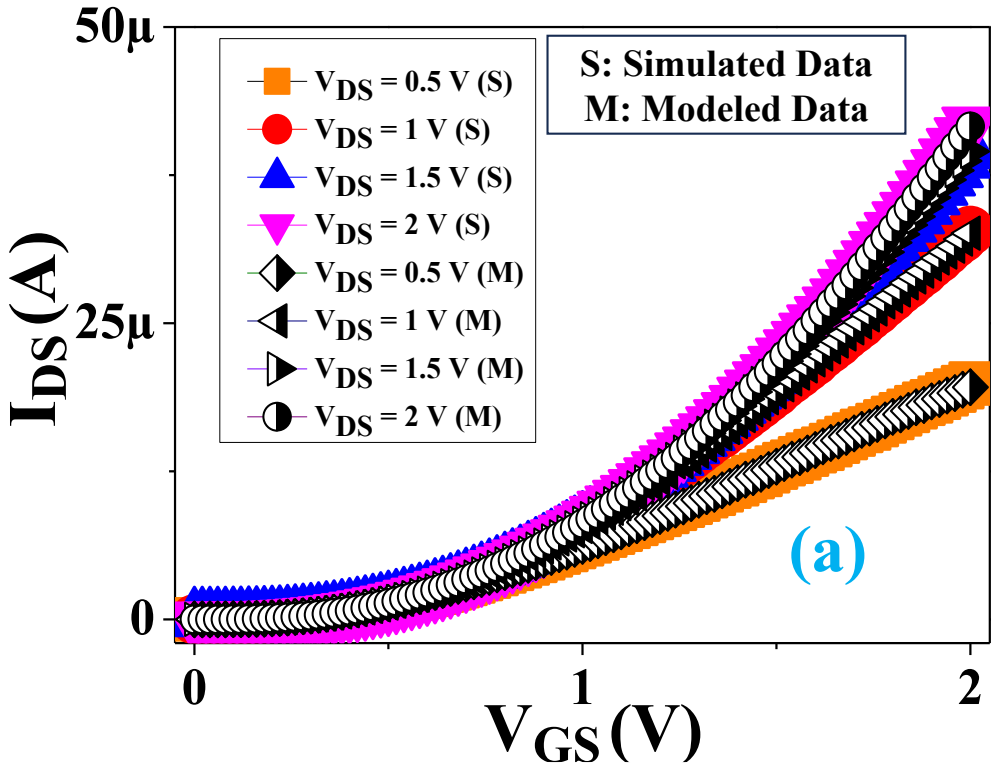


Figure 5.19 (a), (b) Shows the structure, detailed specifications and performance parameters of a-IGZO based "N-TFT" (c), (d) Shows the structure, detailed specifications and performance parameters of PBTTT-C14 based "P-TFT". [95], [99].

Both the devices a-IGZO TFT which is "N-TFT" and PBTTT-C14 based TFT which is "P-TFT" has been compact modeled for both the device characteristics and curves of both simulated/fabricated and modeled data completely superimposes on each other confirm that there is small fraction of error less than 1% is there for these curves.



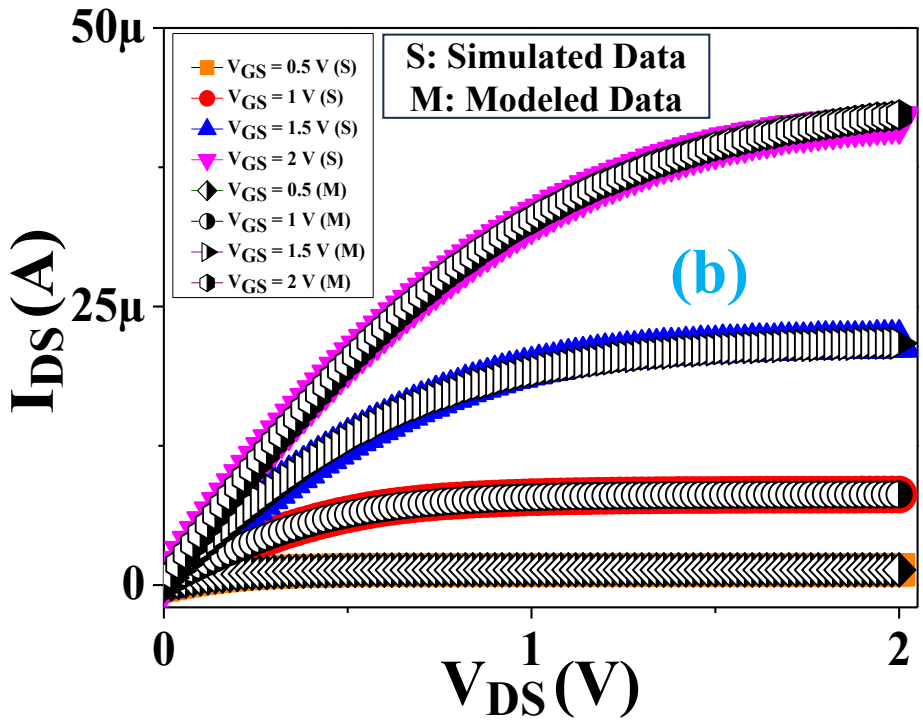
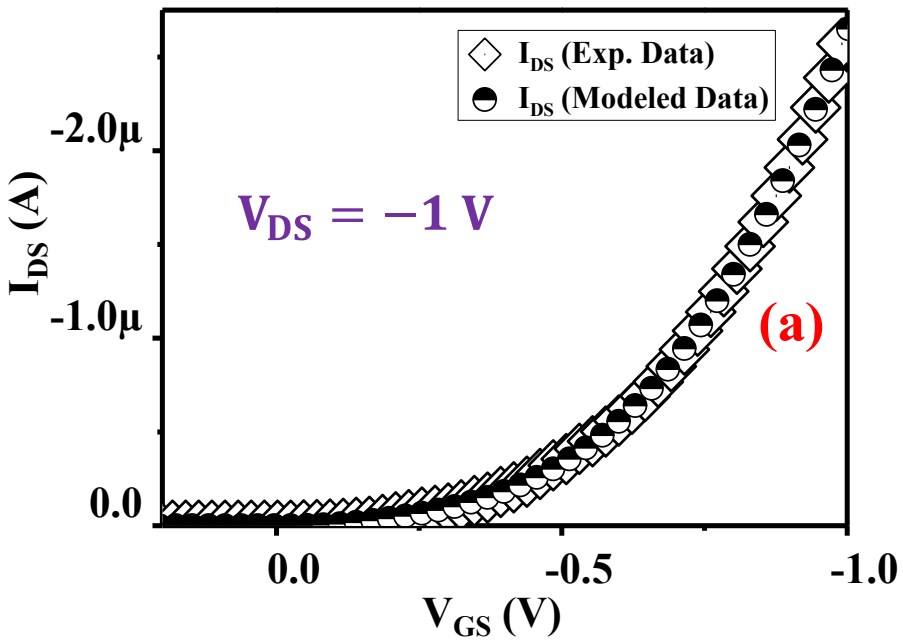


Figure 5.20 (a) Showing the Transfer Characteristics (I_{DS} versus V_{GS}) for V_{DS} varies from 0 to 2 V with an increment of 0.5 V (b) Showing Output Characteristics (I_{DS}) versus (V_{DS}) for V_{GS} varies from 0 to 2 V with an increment of 0.5 V [99].



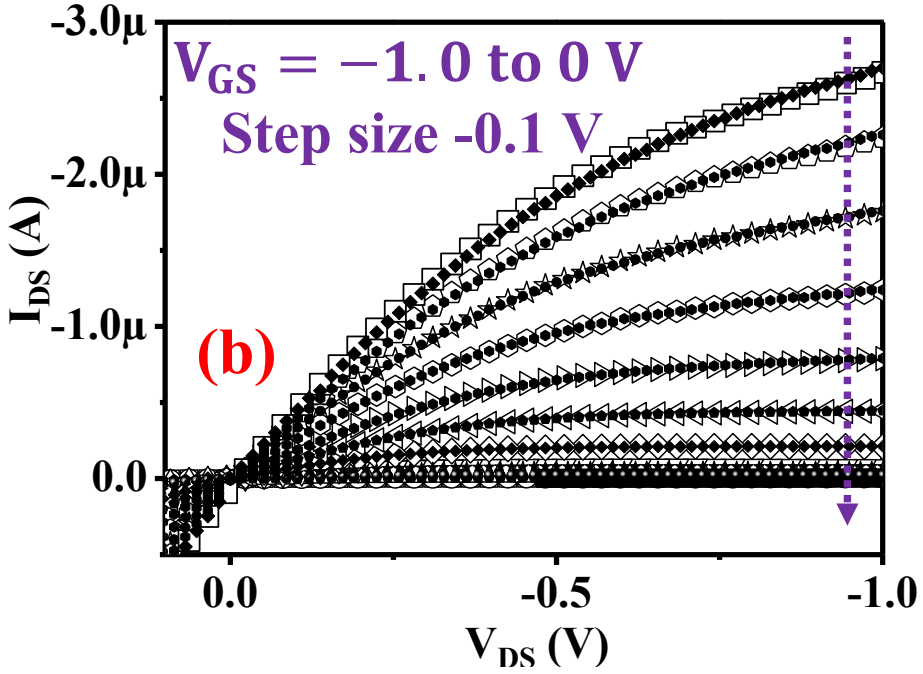


Figure 5.21 (a) Comparison of experimental and modeled data of transfer curve i.e., Drain current – Gate to Source Voltage $(I_{DS} - V_{GS})$ (b) Output characteristics curve i.e., Drain current – Drain to Source Voltage $(I_{DS} - V_{DS})$ for Gate voltage (V_{GS}) varying from 0 to -1V having step size of -0.1 V [95].

In **Figure 5.20 (a)** and **(b)**, device characteristics of a-IGZO based TFT has been shown and in **Figure 5.21 (a)** and **(b)** device characteristics of PBTTT-C14 based TFT has been shown.

5.4 Simulation of Basic Logic Gate Family 2-Input NOR, NAND, AND, OR Circuit, Inverter Circuit and Transient Analysis

At Silvaco-Gateway tool basic libraires exist, which have components as vdd, vpulse, gnd ,etc. In this Silvaco-Gateway platform these compact modeled devices e.g. a-IGZO (N-TFT) and PBTTT-C14 (P-TFT) has been imported for the realization of different analog and digital circuits. Additionally, Smart-Spice Simulator also exist in this tool for analyzing the transient and voltage transfer characteristics which is very helpful for

verifying truth-table, parameter estimation as propagation delay, logic swing, etc. Initially, basic logic gate family as 2-inputs NAND, NOR, AND and OR gates are implemented at Silvaco-Gateway tool using P-TFT [100]. In **Figure 5.22 (a) and (b),** schematic of 2-Input NAND and NOR gates are shown and in **Figure 5.23 (a) and (b),** the circuitry of NAND and NOR gates are implemented using P-TFT.

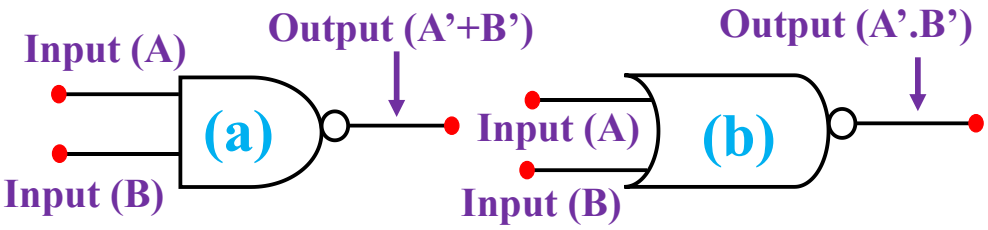


Figure 5.22 (a) and (b) Showing the symbol of 2-inputs NAND and NOR gates.

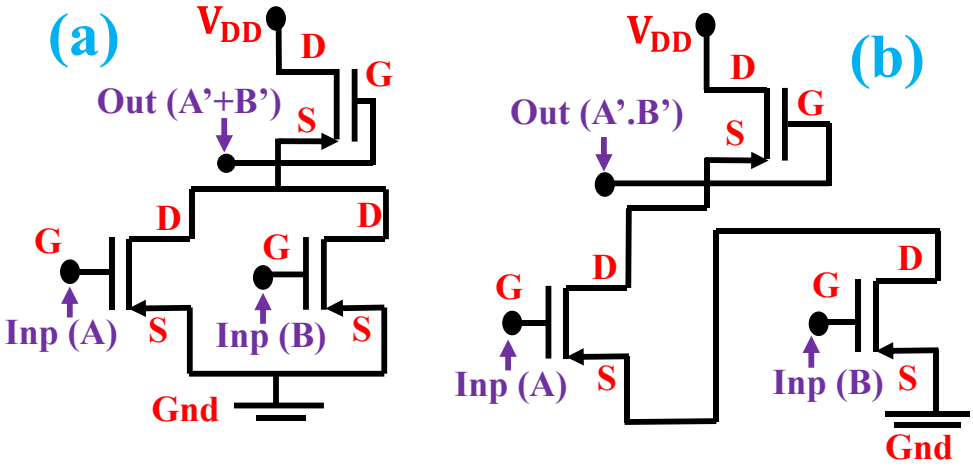


Figure 5.23 (a) and (b) Diagrams showing implementation of 2-inputs NAND and NOR gates using P-TFT.

In order to distinguish between 2 different inputs, inputs voltages are provided as -1.8 and -2 V. As NAND and NOR gates are implemented using P-TFT therefore input voltages -1.8 V and -2 V are considered as logic '0' and 0 V is considered as logic '1'. In **Figure 5.24 (a) and (b)**, transient analysis is done for 2-inputs NAND gate and corresponding

truth table is verified in which all the 4 cases as 00,11,01,10 and their respective outputs as 1,0,1,1 are mentioned in it.

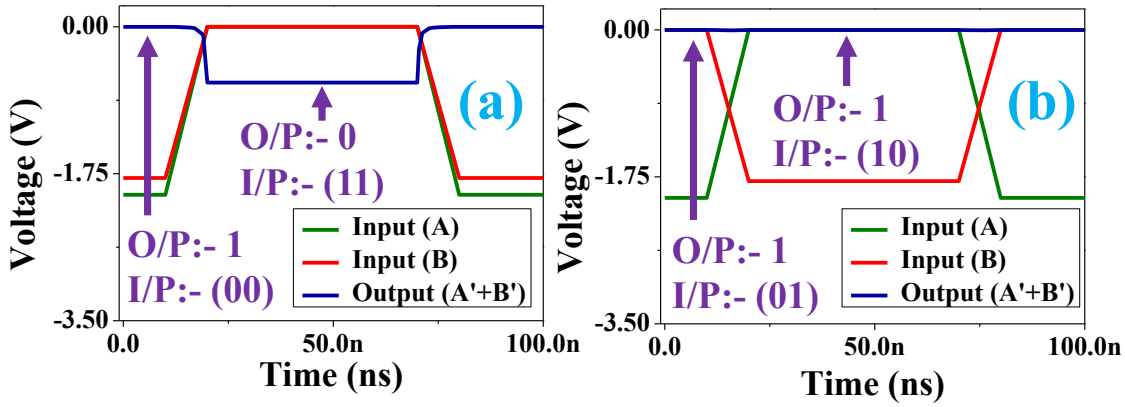


Figure 5.24 (a) and (b) Indicating the truth table of 2-Inputs NAND gate which is analysed with the help of Smart-Spice Simulator.

Similarly for 2-inputs NOR gate transient analysis and corresponding truth table for all 2-inputs as 00,01,10,11 is verified which is shown in **Figure 5.25 (a) and (b)** as 1,0,0 and 0 as output. As "NAND" and "NOR" are universal gates, therefore with the help of these universal gates, "OR" and "AND" gates are implemented

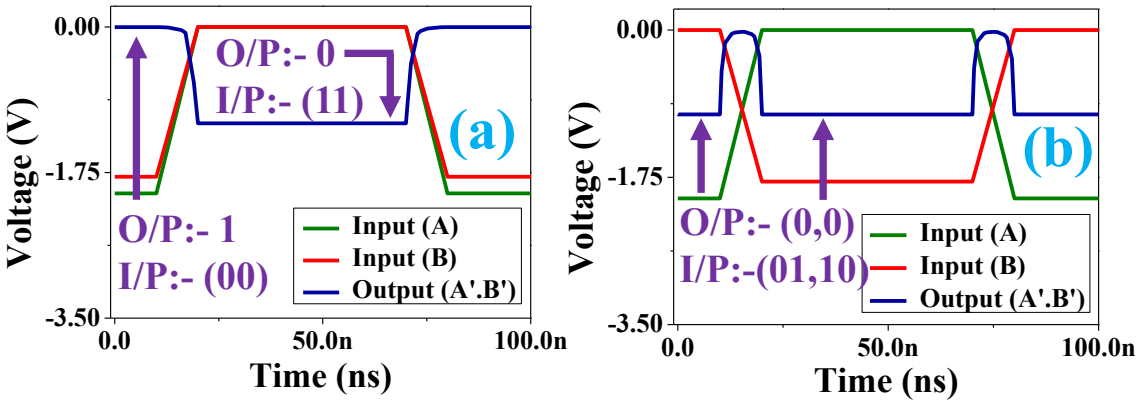


Figure 5.25 (a) and (b) Indicating the truth table of 2-Inputs NOR gate which is analysed with the help of Smart-Spice Simulator.

Since 2-inputs “NAND” and “NOR” are already realized and verified which are seen above in **Figure 5.24 and 5.25 (a, b).**

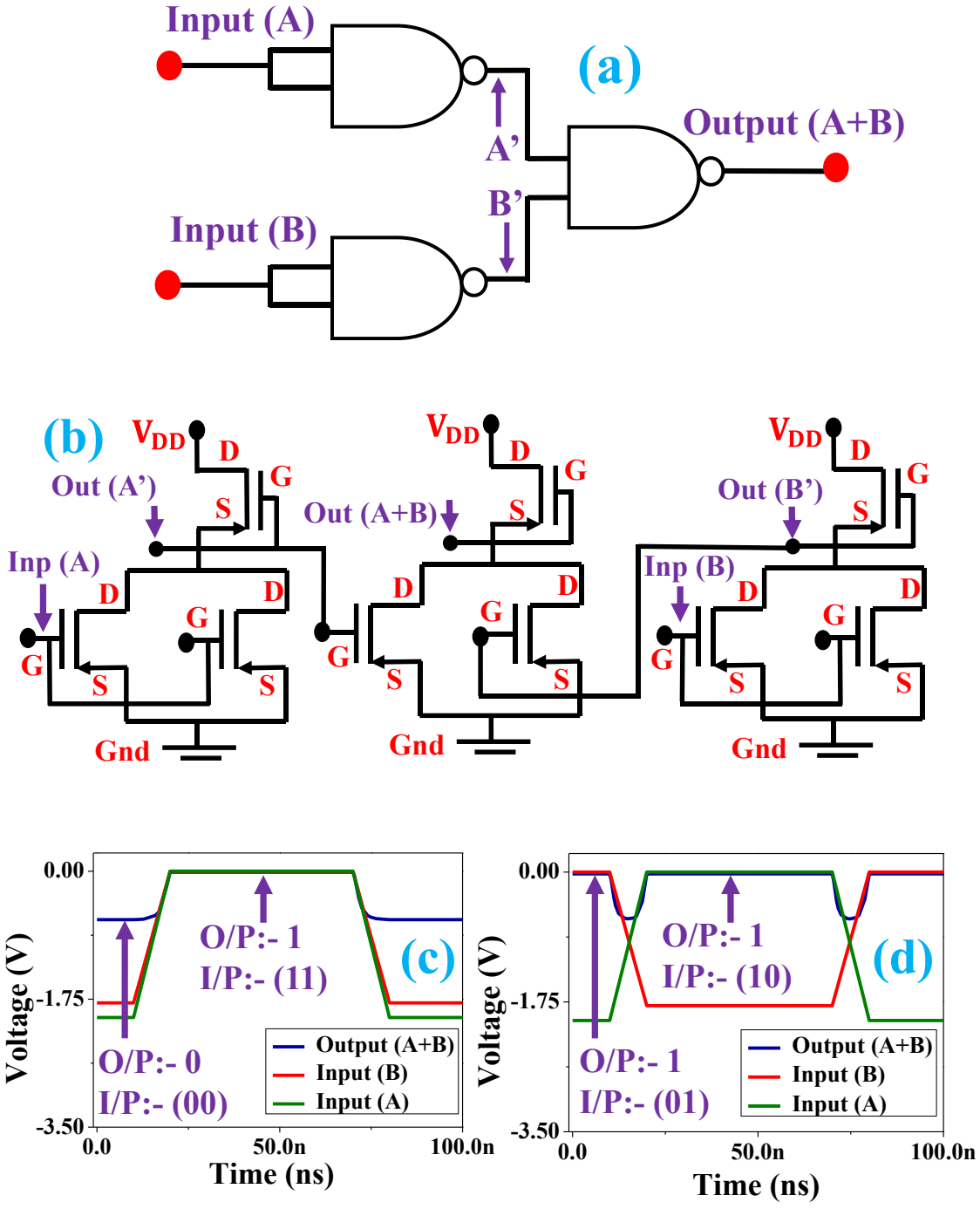
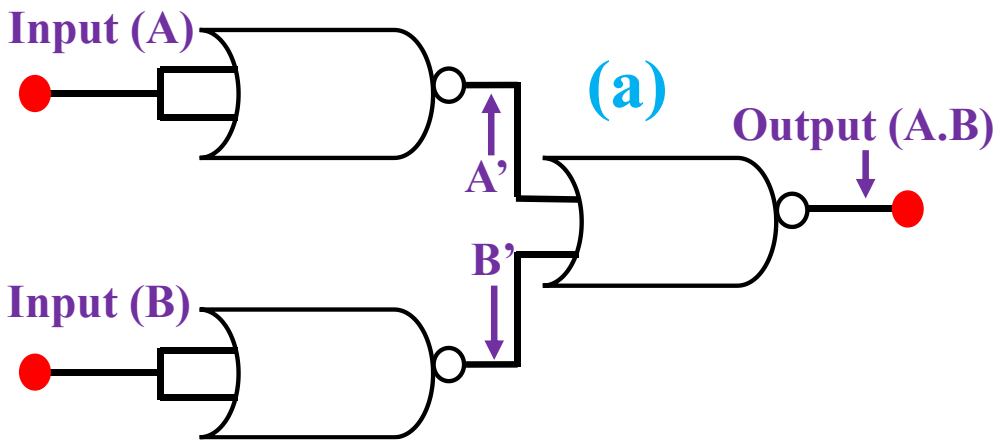


Figure 5.26 (a) Showing schematic of OR gate implementation using 2-input NAND gate (b) Circuitry of OR gate implemented using 2-input NAND gate at Silvaco-Gateway platform. (c), (d) Indicating truth tables of OR gate which is analyzed with the help of

smart-spice simulator.

In **Figure 5.26 (a)** schematic of "OR" gate is shown where it is developed with the help of 3 NAND (2-inputs) gates arranged to generate output as "A+B". Similarly in **Figure 5.26 (b)** Circuitry of "OR" gate which is mentioned in **Figure 5.26 (a)** is implemented at Silvaco-Gateway platform and its corresponding transient analysis is performed which resulted helpful in realizing its respective truth table mentioned in **Figure 5.26 (c)** and **Figure 5.26 (d)**, in these two figures all the 4 cases for 2-inputs as 00,11,10 and 01 and output according to it 0,1,1 and 1 are verified. For realizing "AND" gate with the help of 2-inputs NOR gates the schematic of its related circuitry is mentioned in **Figure 5.27 (a)** in which 3 NOR gates (2- inputs) are arranged to realize "AND" operation to produce output as "A.B". According to the schematic of the circuitry mentioned in **Figure 5.27 (a)**, the same circuitry of AND gate is implemented at Silvaco-Gateway platform mentioned in **Figure 5.27 (b)**. Similarly, its transient analysis is also performed by the means of which its truth table is also verified which is mentioned in **Figure 5.27 (c) and Figure 5.27 (d).** Using these two figures all the 4 cases of 2-inputs as 00,01,10,11, and its corresponding output as 0,0,0 and 1 is verified.



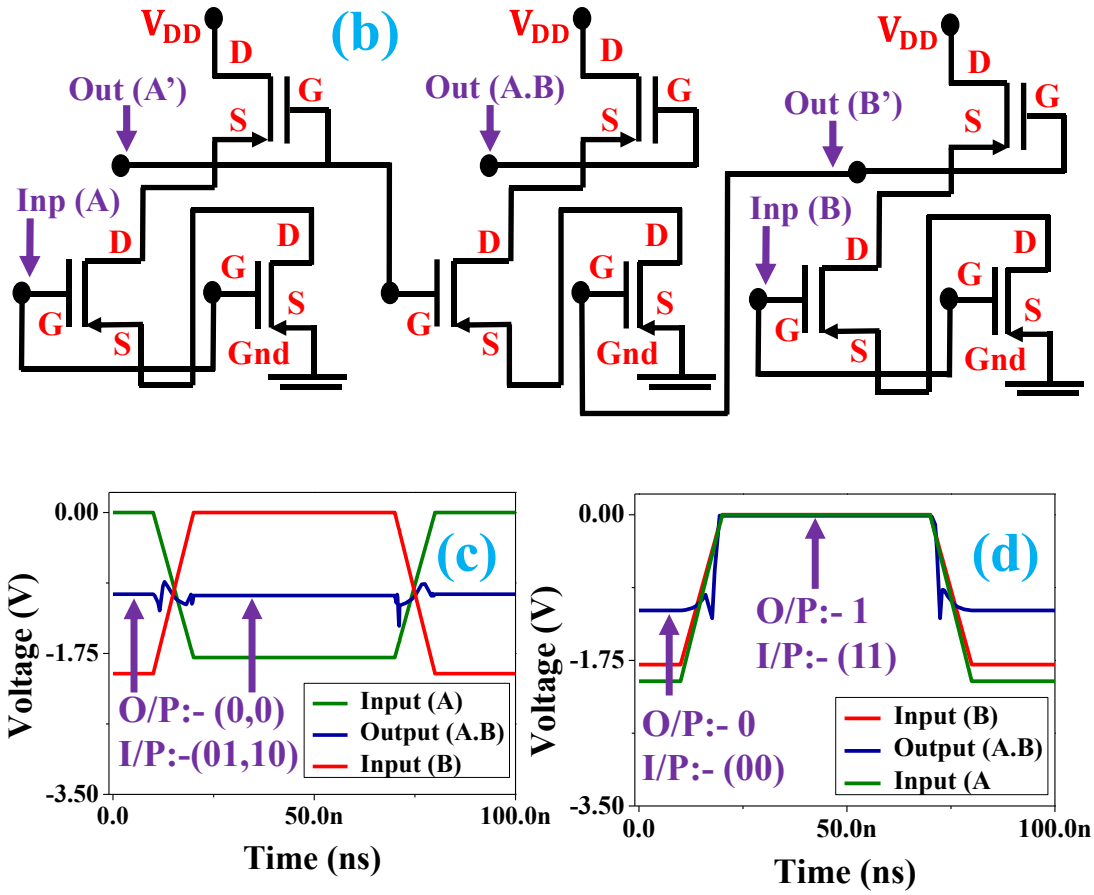
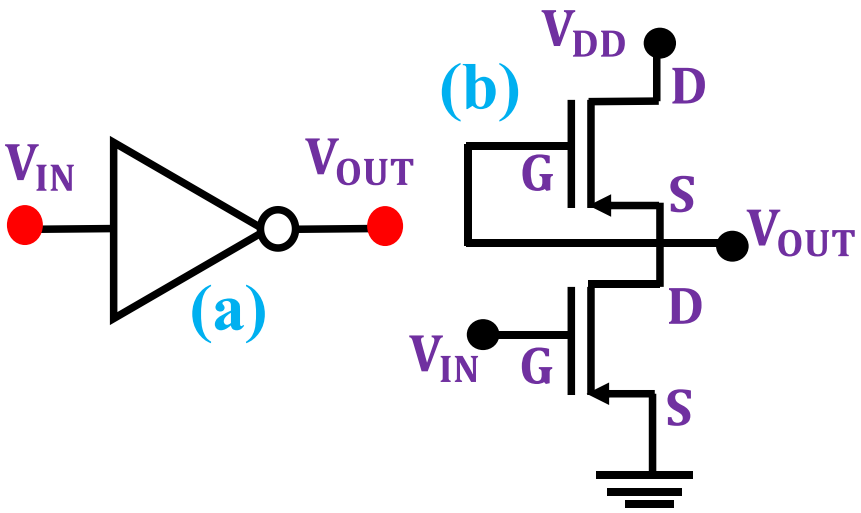


Figure 5.27 (a) Showing schematic of AND gate implementation using 2-input NOR gate (b) Circuitry of AND gate implemented using 2-Input NOR gate at Silvaco-Gateway platform. (c), (d) Indicating truth tables of AND gate which is analyzed with the help of smart-spice simulator.



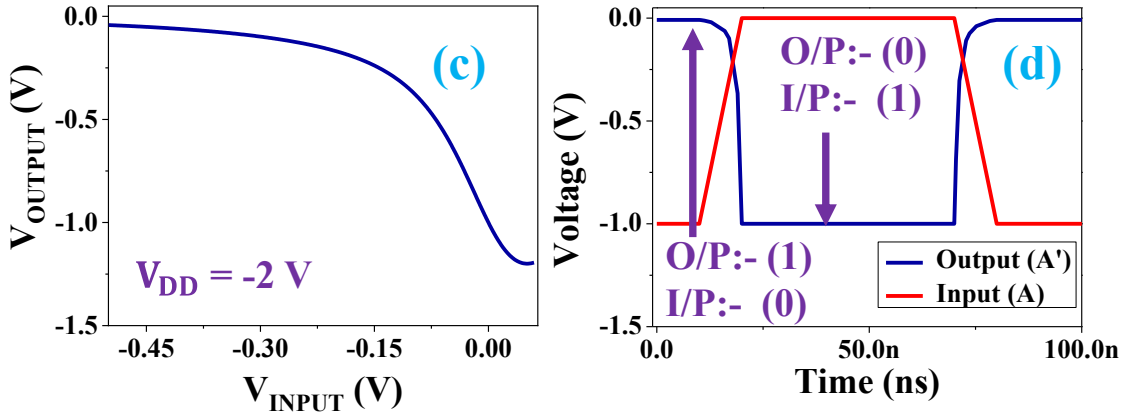


Figure 5.28 (a) and (b) Showing the symbol of NOT gate and NOT gate circuit diagram using P-TFT [240] (c), (d) Indicating truth-table and voltage transfer characteristics of NOT gate respectively [240].

In **Figure 5.28 (a) and (b)** NOT gate is implemented using P-TFT and respective DC, transient analysis is performed mentioned in **Figure 5.28 (c) and (d)**. These analysis helps in evaluating parameters as average propagation delay (τ_P) = 3.7ns, inverter gain ~ 4.7 and logic swing of 1.18V respectively. **Table 5.1** presents all the cases, ranging from 00 to 11, with the results closely aligning with the expected values. A small fraction of error, less than 1%, was observed.

Table 5.1 Truth Table of All Implemented Logic Gates

Input	AND Gate Output (V)	OR Gate Output (V)	NAND Gate Output (V)	NOR Gate Output (V)
00	-1.15 ~ 0	-0.66 ~ 0	-0.002 ~ 1	-0.001 ~ 1
01	-1.01 ~ 0	-0.02 ~ 1	-0.004 ~ 1	-1.002~ 0
10	-1.01 ~ 0	-0.02 ~ 1	-0.004 ~ 1	-1.002 ~ 0
11	-0.01 ~ 1	-0.01 ~ 1	-0.66 ~ 0	-1.158 ~ 0

5.5 Simulation of CMOS Inverter Circuit and Transient, DC Analysis

On successful implementation of basic logic gate family, CMOS Inverter circuit is implemented which is shown in **Figure 5.29**.

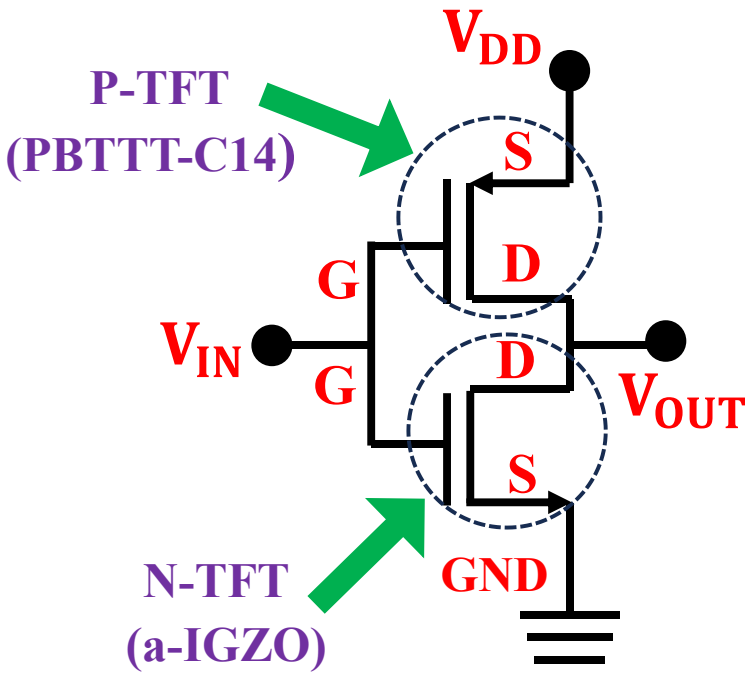
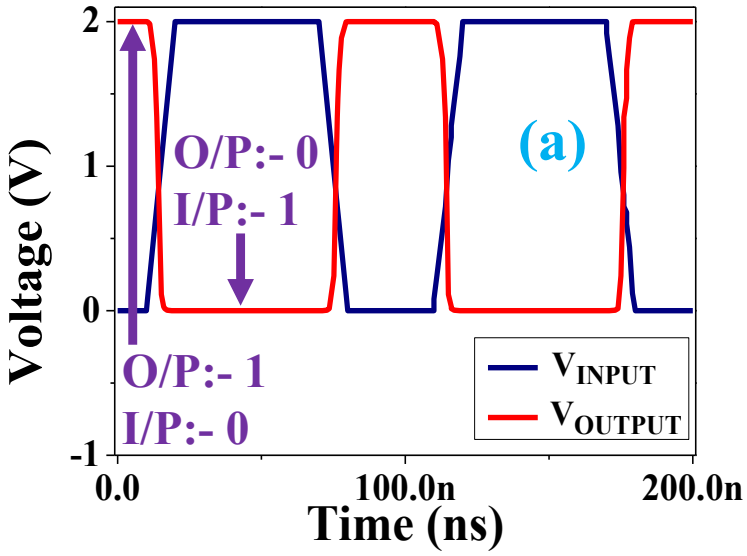


Figure 5.29 Shows the circuit of CMOS Inverter in which a-IGZO used as N-TFT and PBTTT-C14 acted as P-TFT.

The CMOS inverter circuit is essential for the implementation of various analog circuits and amplifiers, as discussed in [241], [242] .



In order to verify the nature of inverter circuit in which for input "0" the output tends to "1" and vice-versa. Transient and DC Characterization has been performed to estimate

the propagation delay, voltage gain, logic swing which is shown in **Figure 5.30 (a) and (b).**

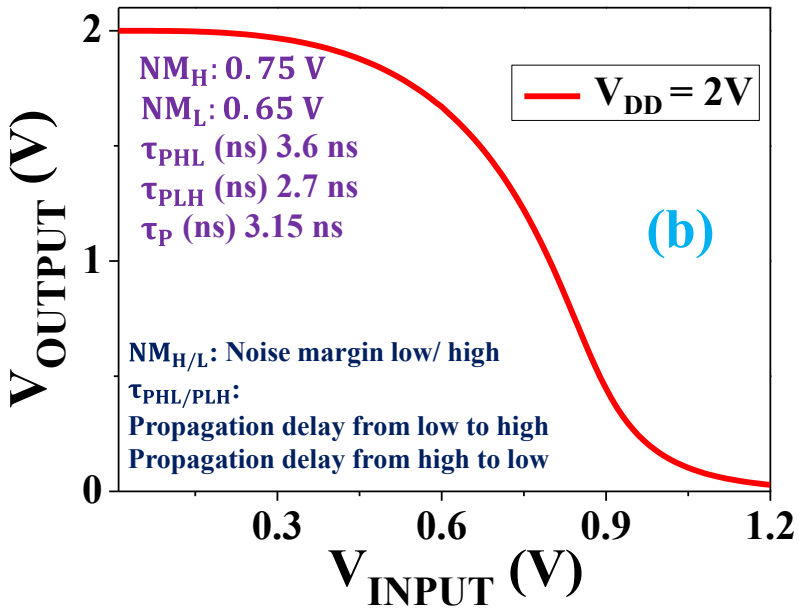


Figure 5.30 (a) and (b) Show the Transient and DC behaviour of CMOS Inverter Circuit.

With the help of Transient and DC behaviour shown in **Figure 5.30 (a) and (b)**, there are list of Parameters estimated which is shown in **Table 5.2**.

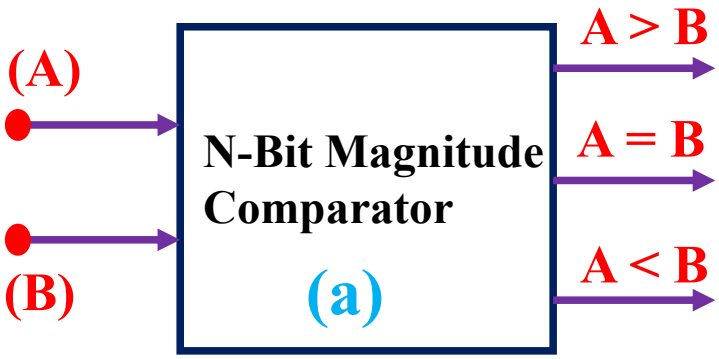
Table 5.2 List of Evaluated Parameters

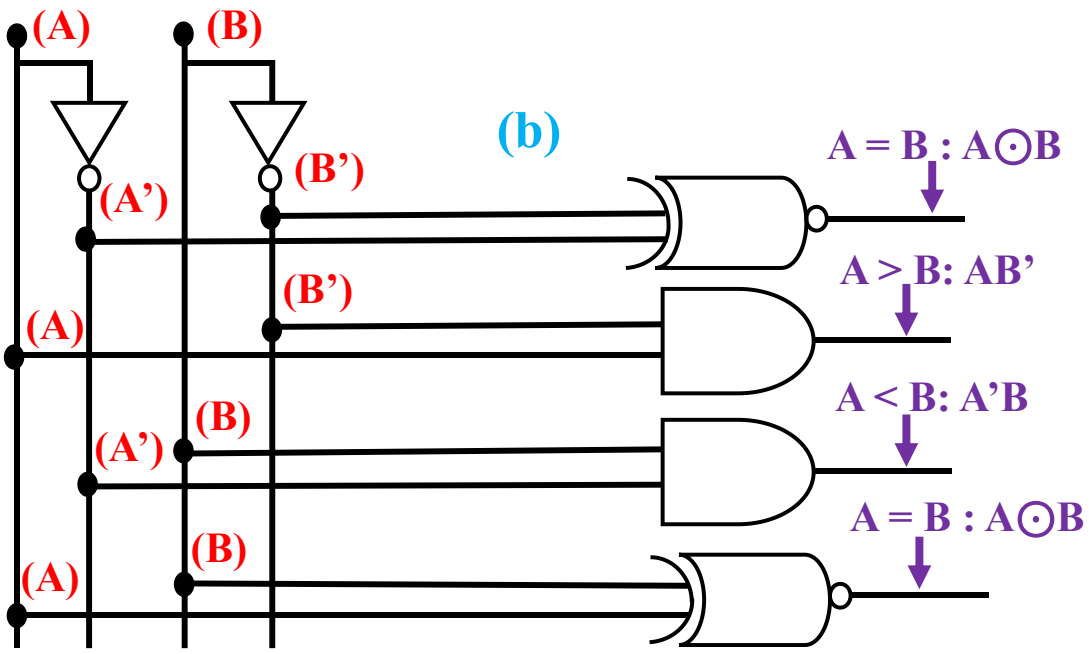
S.No.	Parameter Name	Corresponding Value
1.	τ_{PHL} (ns)	3.6 ns
2.	τ_{PLH} (ns)	2.7 ns
3.	τ_P (ns)	3.15 ns
4.	Inverter Gain (V)	9.1
5.	Inverter Input (V) (2 V)	Output (9.7E-08)
6.	Inverter Input (V) (0 V)	Output (2V)
7.	Logic Swing (V)	2 V

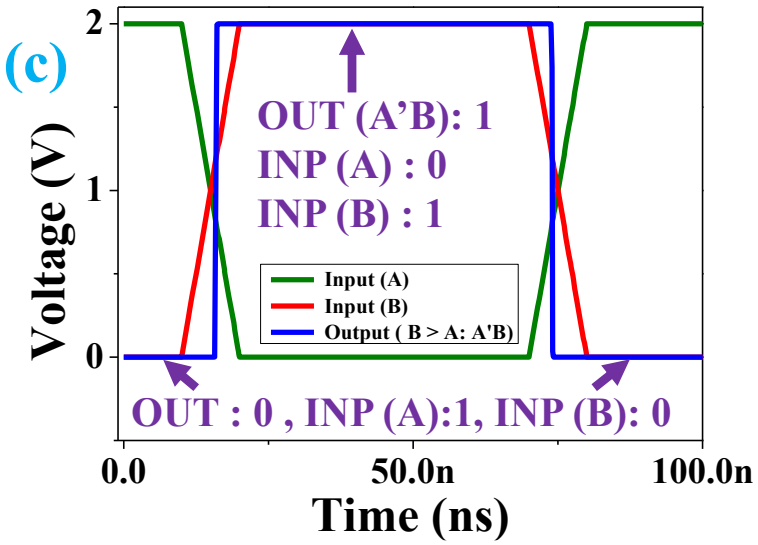
5.6 Simulation of 1-Bit Magnitude Comparator Circuit and Transient Analysis

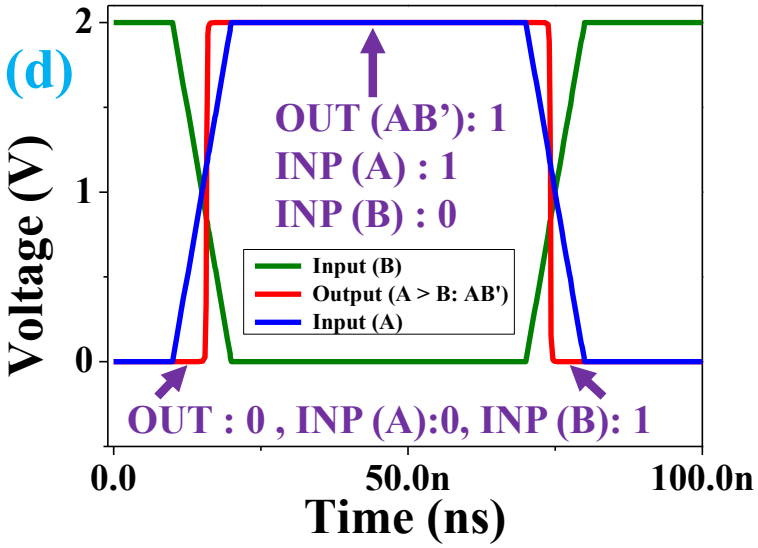
The CMOS logic was successfully employed to implement the inverter circuit, and all associated parameters were calculated. Additionally, this CMOS logic was used to

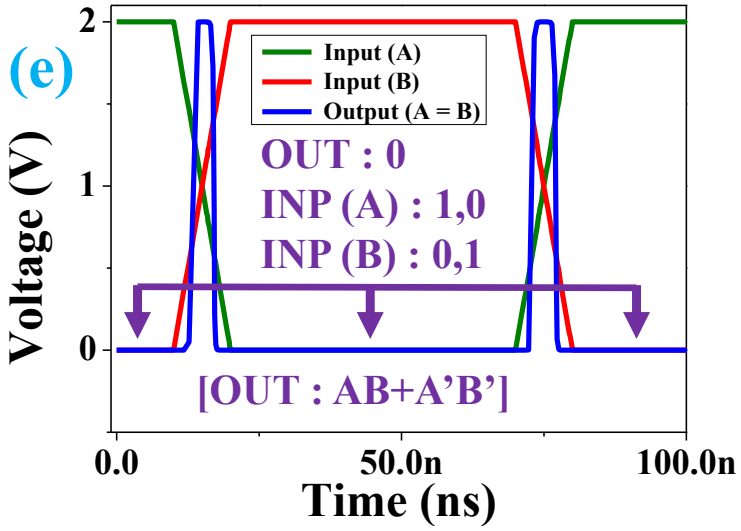
implement a 1-bit magnitude comparator. A magnitude comparator evaluates two binary numbers to determine whether one is greater, lesser, or if they are equal. Comparators are critical components in arithmetic logic units (ALUs), data sorting, and various computational processes [243]–[245]. In **Figure 5.31 (a) and (b)**, the circuit diagram of the 1-bit magnitude comparator is depicted, illustrating the realization of the circuitry using logic gates [96]. **Figure 5.31 (c)** shows the scenario for the case when A < B. For inputs A and B, when A is 0 and B is 1, the output is 1; for all other input combinations, the output remains 0. Similarly, **Figure 5.31 (d)** verifies the case when A > B. When A is 1 and B is 0, the output is 1; for all other combinations, the output is 0.






(c)
Voltage (V)
2
1
0
OUT (A'B): 1
INP (A) : 0
INP (B) : 1
Input (A)
Input (B)
Output (B > A: A'B)
OUT : 0 , INP (A):1, INP (B): 0
0.0
50.0n
100.0n
Time (ns)


(d)
Voltage (V)
2
1
0
OUT (AB'): 1
INP (A) : 1
INP (B) : 0
Input (B)
Output (A > B: AB')
Input (A)
OUT : 0 , INP (A):0, INP (B): 1
0.0
50.0n
100.0n
Time (ns)


(e)
Voltage (V)
2
1
0
Input (A)
Input (B)
Output (A = B)
OUT : 0
INP (A) : 1,0
INP (B) : 0,1
[OUT : AB+A'B']
0.0
50.0n
100.0n
Time (ns)

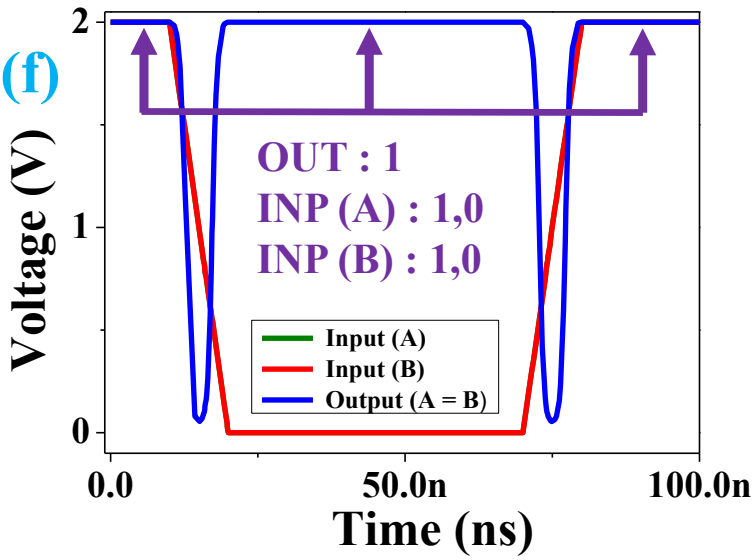


Figure 5.31 (a) Displays the block diagram of the comparator circuit. (b) presents the equivalent diagram of the 1-bit magnitude comparator implemented using logic gates. (c), (d), (e) and (f) exhibit the transient behavior for all three cases of the 1-bit magnitude comparator: (A < B) , (A > B) and (A = B).

In **Figure 5.31 (e-f)**, the equality case (A = B) is demonstrated. The output behaviour mirrors the XNOR gate operation, where the output is 1 only when both inputs are identical; otherwise, the output is 0. The transient behaviour of this 1-bit magnitude comparator shown in **Figure 5.31 (c-f)** verifies the truth table for all 4 cases i.e. 00,01,10,11.**Table 5.3** summarizes the output values for all possible cases: A > B, A < B, and A= B, based on the corresponding input values of A and B. For input logic (00) and (11), the output is 2V, indicating a logic '1', thus confirming the equality case A=B. Similarly, for input logics (01) and (10), the output is also logic '1'. Input values of 2V and 0V for A and B represent logic '1' and '0', respectively, with an output of 2V corresponding to logic '1'. Therefore, across all input cases from 00 to 11, the outputs for A > B, A < B, and A = B are verified, confirming that the CMOS logic is fully suitable for designing a 1-bit magnitude comparator.

Table 5.3 Truth Table of 1-Bit Magnitude Comparator

Input Logic	Input A (V)	Input B (V)	Output (V)
00	0 ~ "0"	0 ~ "0"	2 ~ "1" (A = B) ~ 1
01	0 ~ "0"	2 ~ "1"	2 ~ "1" (A < B) ~ 1
10	2 ~ "1"	0 ~ "0"	2 ~ "1" (A > B) ~ 1
11	2 ~ "1"	2 ~ "1"	2 ~ "1" (A = B) ~ 1

5.7 Simulation of Half Adder Circuit and Transient Analysis

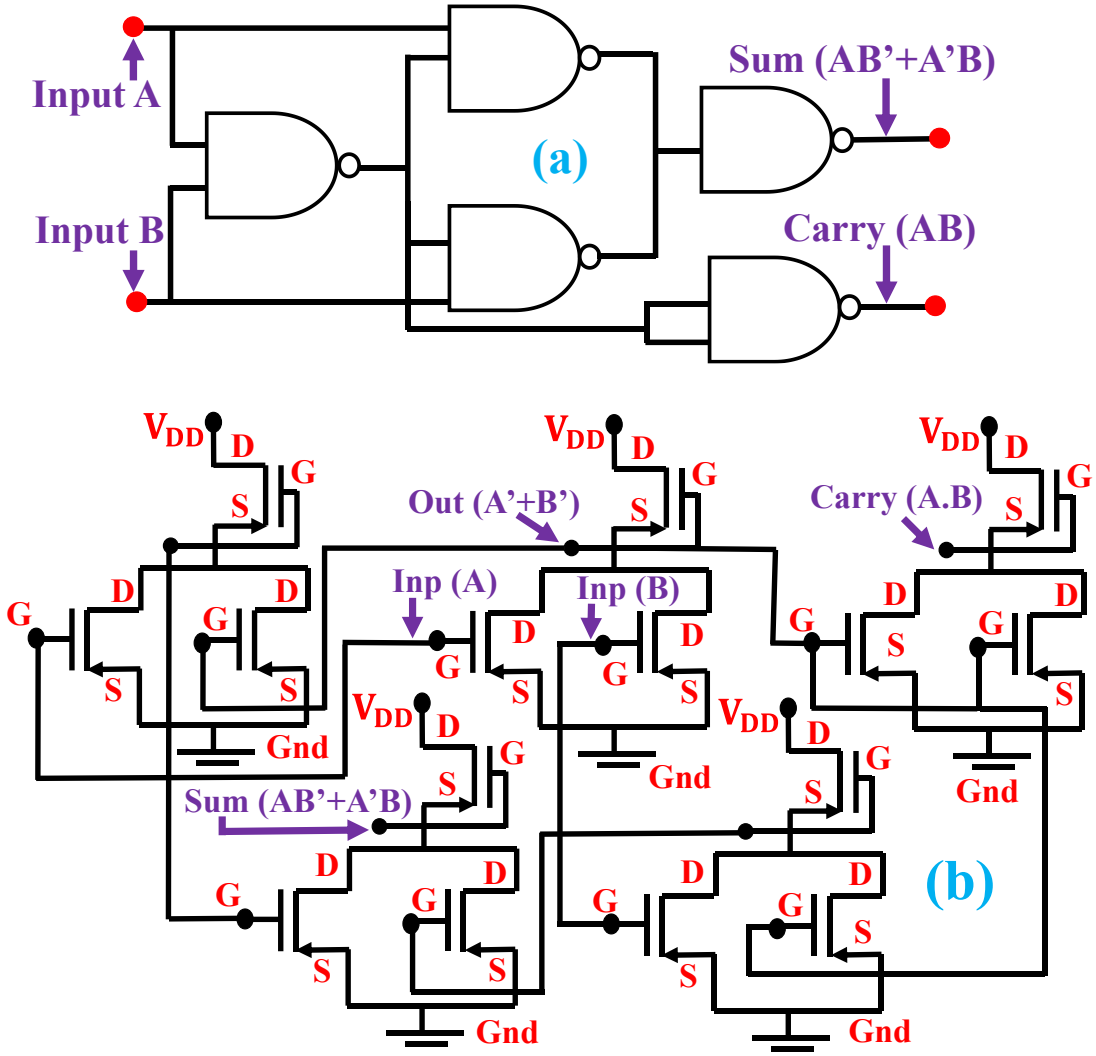


Figure 5.32 (a) Displays the circuit diagram of a half-adder using 2-input NAND gates. (b) Indicates the circuitry of the half-adder implemented using P-TFTs, realized on the Silvaco-Gateway platform.

The half-adder is a combinational circuit used for adding two binary numbers and produces two outputs: 'Sum' and 'Carry.' It is a crucial component in arithmetic logic units (ALUs), floating-point unit multipliers (FPUs), and filter designs [94], [246]. The circuitry of the half-adder is illustrated in **Figure 5.32 (b)**, where the 'Sum' and 'Carry' outputs are expressed in terms of the input variables A and B as follows:

$$Sum = AB'+A'B \qquad (5.1)$$

$$Carry = A.B \qquad (5.2)$$

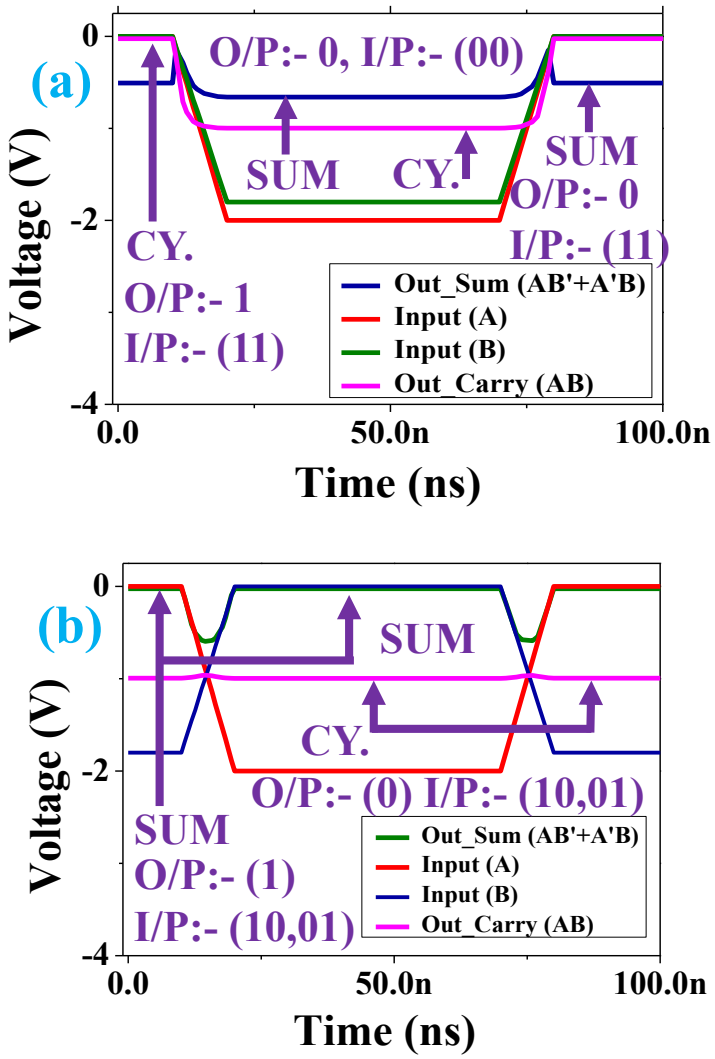


Figure 5.33 (a) and (b) present the truth tables for the Half-Adder Circuit.

Using the Silvaco-Gateway tool and the Smart-Spice Simulator, transient analysis is conducted to verify the truth table of the half-adder and the corresponding outputs. The results for all inputs are displayed in **Figure 5.33 (a) and (b)** and summarized in **Table 5.4**.

Table 5.4 Shows Truth Table of the Half Adder Circuit

S.No.	Input Logic	Output Sum (V) (Sum: AB'+A'B)	Output Carry (V) (Carry: AB)
1.	00	-0.66 ~ '0'	-0.99 ~ '0'
2.	01	-0.02 ~ '1'	-0.99 ~ '0'
3.	10	-0.02 ~ '1'	-0.99 ~ '0'
4.	11	-0.51 ~ '0'	-0.02 ~ '1'

5.8 Simulation of 4:1 Multiplexer For Realizing It As Universal Gate and Transient Analysis

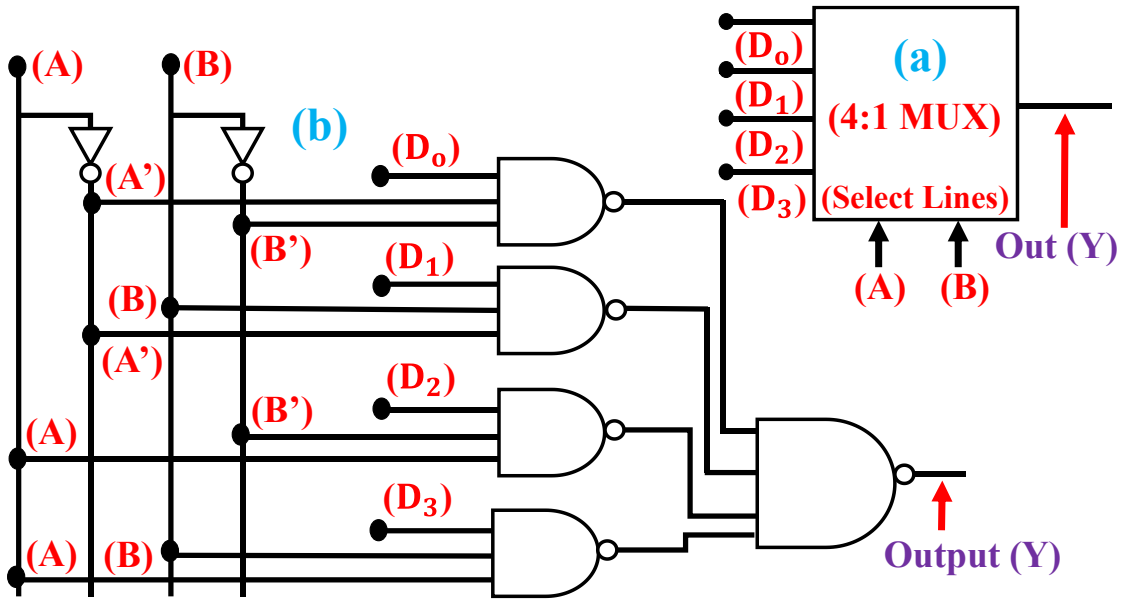
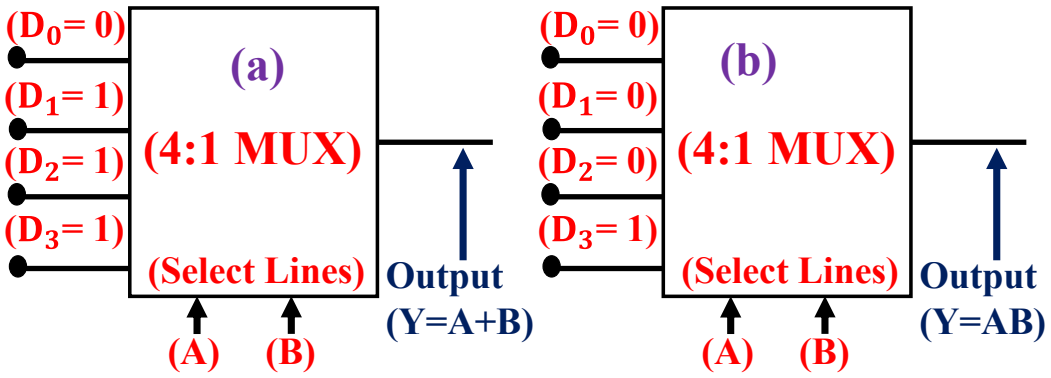
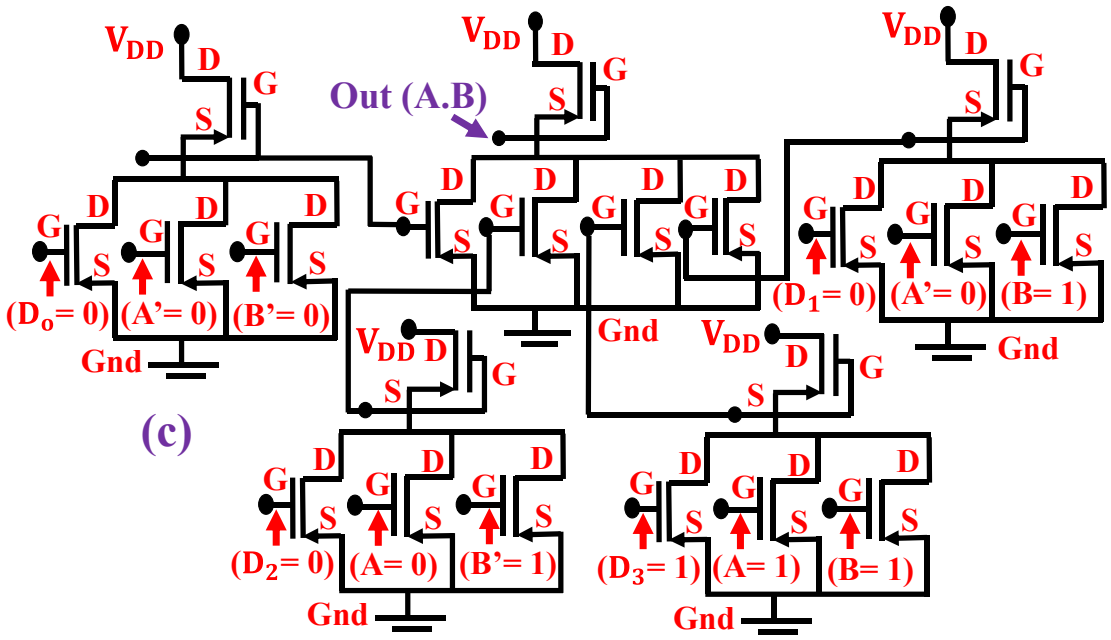


Figure 5.34 (a) Showing the block diagram of 4:1 Multiplexer (b) Showing the internal circuitry of 4:1 Multiplexer.

In this section, 4:1 Multiplexer is implemented which will be further used to realize logic gates such as AND, OR, XOR, and XNOR. Using multiplexers all logic functions can be

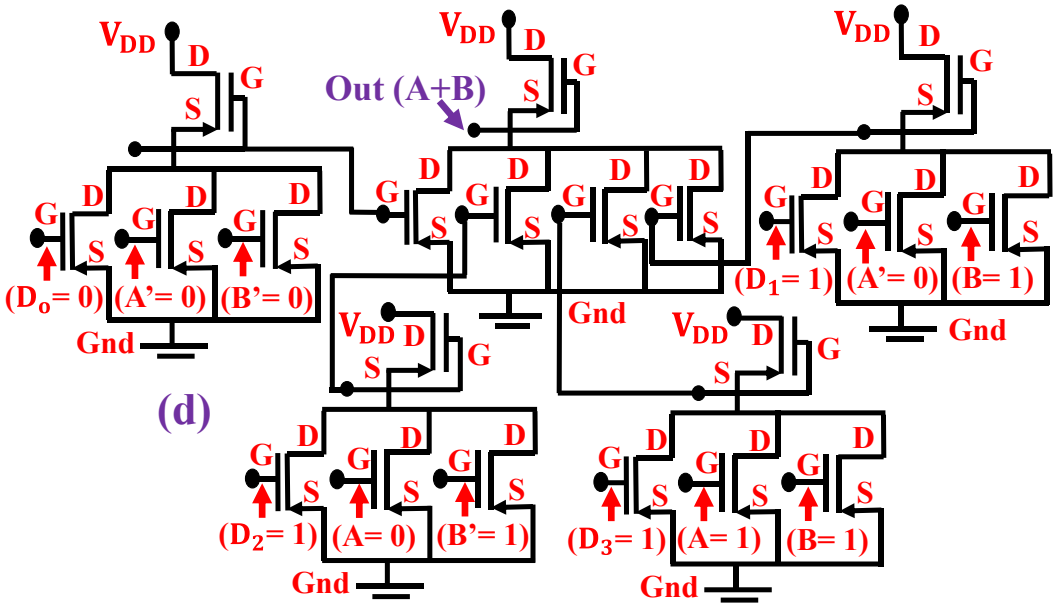
realized [247], [248]. Furthermore, the 4:1 multiplexer circuit is expected to be used in the development of higher-order multiplexer circuits, ALU circuits, and other complex systems. In Figure 5.34 (a) block diagram of 4:1 Multiplexer is displayed, Figure 5.34 (b) the complete circuit of 4:1 Multiplexer is shown where $\mathbf{D_0}, \mathbf{D_1}, \mathbf{D_2}$ and $\mathbf{D_3}$ are the 4 inputs and A and B are the select lines.





As the multiplexer belongs to the family of universal gates, it can be further utilized to implement various logic circuits. **Figure 5.35 (c) and (d)** exhibit the circuitry of the 4:1 multiplexer, implemented to realize logic gates such as “AND” and “OR”.

The corresponding transient analysis has been performed, and the resulting truth tables are verified, as displayed in **Figure 5.35 (e) and (f)**.



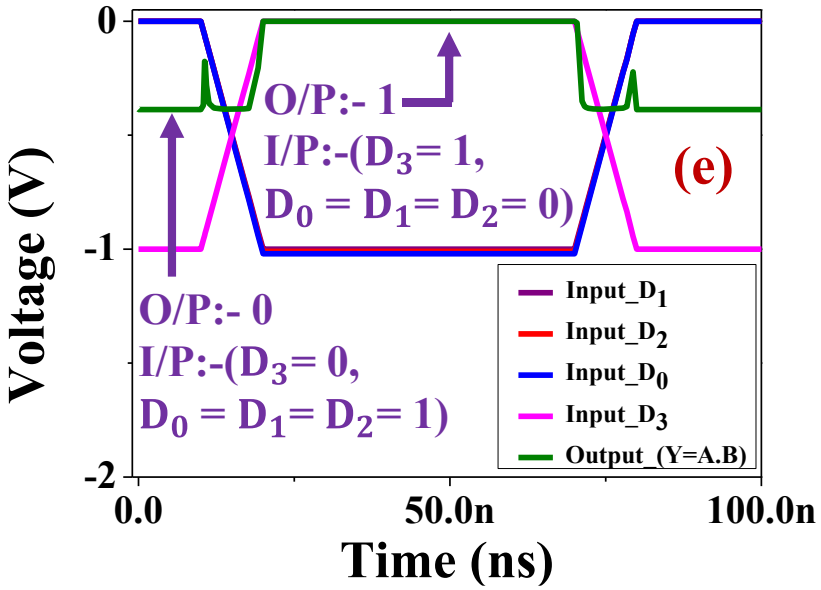


Table 5.5 Shows Truth Table of "AND" Logic Gate Circuit

Input	Input Value (V)	Output Value (V) (Y=A.B)	Input Value (V)	Output Value (V) (Y=A.B)
D_0 (00)	-0.04 ~ 1	-0.37 ~ 0	-0.96 ~ 0	-0.007 ~ 1
D_1 (01)	-0.04 ~ 1	-0.37 ~ 0	-0.96 ~ 0	-0.007 ~ 1
D_2 (10)	-0.04 ~ 1	-0.37 ~ 0	-0.96 ~ 0	-0.007 ~ 1
D_3 (11)	-0.96 ~ 0	-0.37 ~ 0	-0.04 ~ 1	-0.007 ~ 1

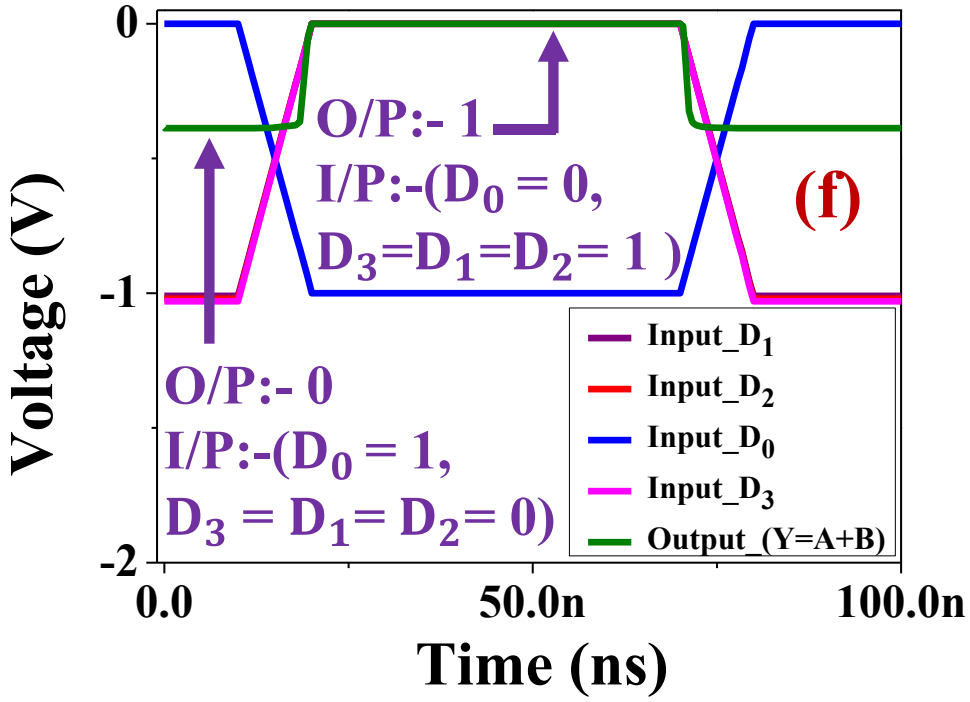


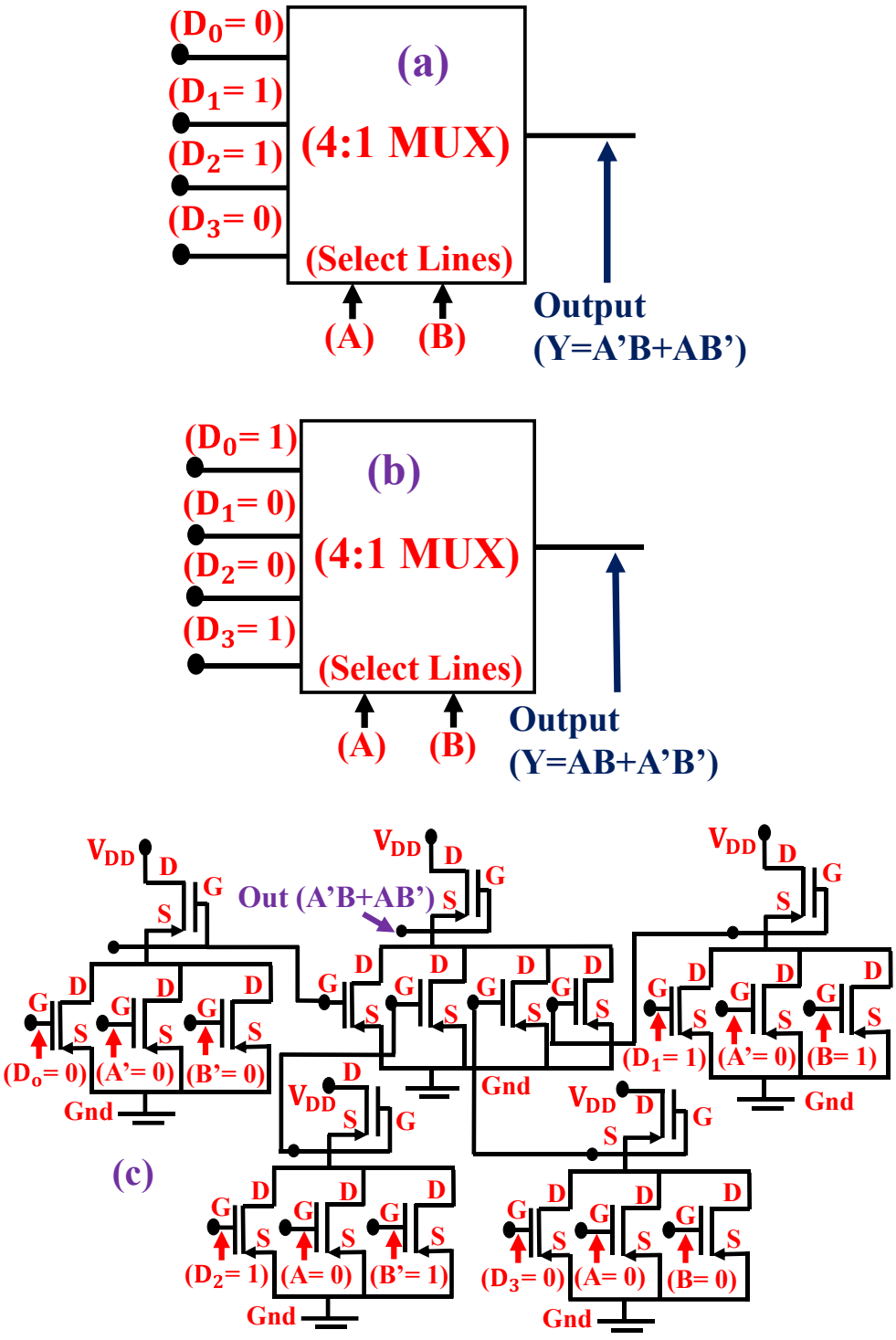
Figure 5.35 (a), (b) Show the implementation of "OR" and "AND" gate using 4:1 Multiplexer (c), (d) Present the complete circuitry of realizing "AND", "OR" gate with the help of 4:1 Multiplexer on Silvaco-Gateway tool (e), (f) Display the truth tables of "AND" and "OR" gates, analyzed using the smart-spice simulator.

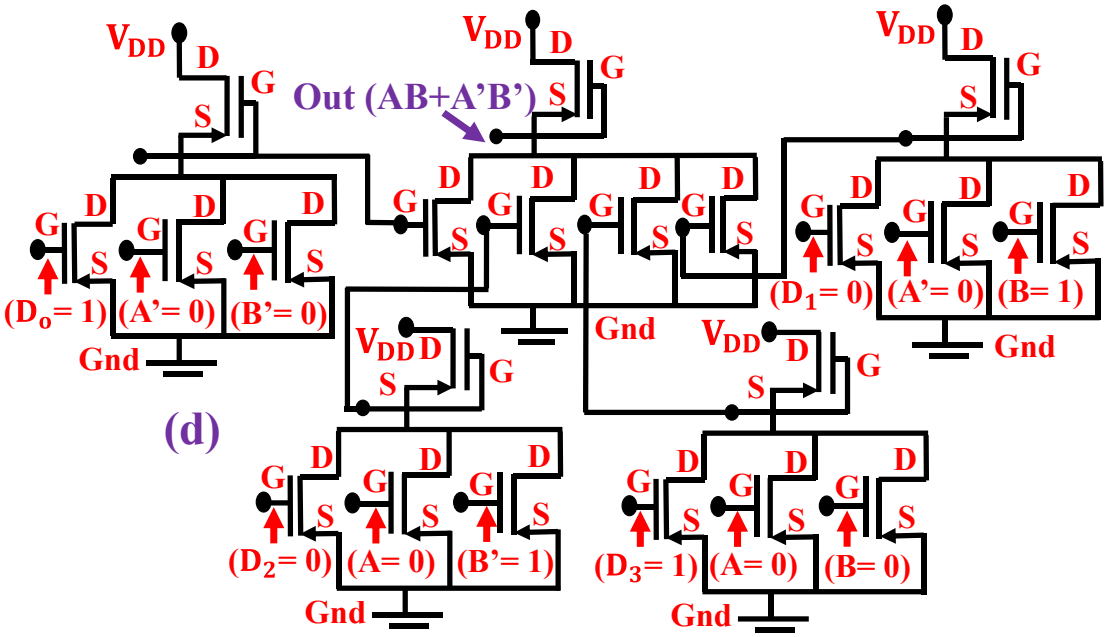
Table 5.6 Shows Truth Table of "OR" Logic Gate Circuit

Input	Input Value (V)	Output Value (V) (Y=A+B)	Input Value (V)	Output Value (V) (Y=A+B)
D_0 (00)	-0.04 ~ 1	-0.39 ~ 0	-0.96 ~ 0	-0.008 ~ 1
D_1 (01)	-0.97 ~ 0	-0.39 ~ 0	-0.04 ~ 1	-0.008 ~ 1
D_2 (10)	-0.98 ~ 0	-0.39 ~ 0	-0.04 ~ 1	-0.008 ~ 1
D_3 (11)	-0.99 ~ 0	-0.39 ~ 0	-0.04 ~ 1	-0.008 ~ 1

In **Tables 5.5** and **5.6**, the truth tables of "OR" and "AND" gates are presented, confirming the successful implementation of these logic gates. In the above case, **Figure 5.35** shows that the "OR" and "AND" logic gate circuits were realized and verified using

the implemented 4:1 multiplexer. Similarly, following the same approach, tools, and methodology, the "XOR" and "XNOR" logic gate circuits were implemented. Their respective transient analyses and truth tables were verified, as shown in **Figure 5.36 (c–e)** and **Tables 5.7 and 5.8**.





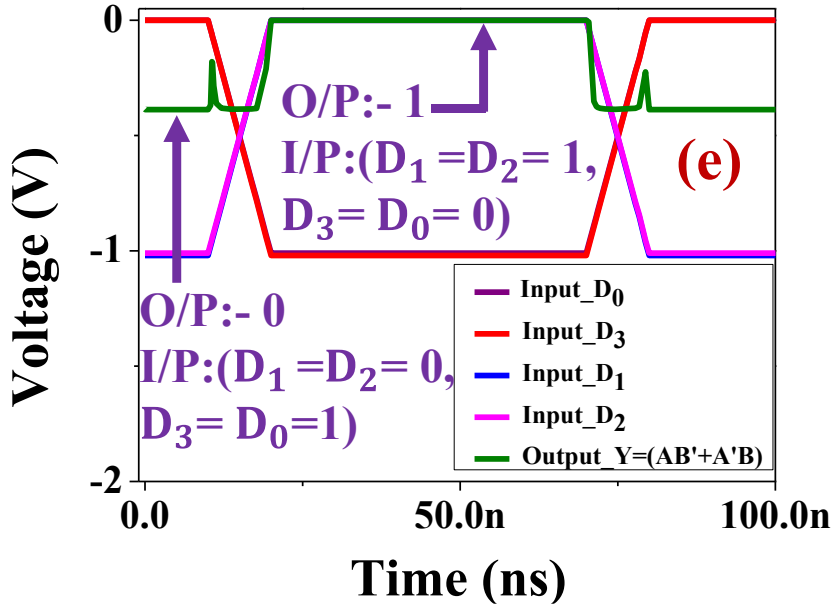


Table 5.7 Shows Truth Table of "XOR" Logic Gate

Input	Input Value (V)	Output Value (V) (Y=A⊕B)	Input Value (V)	Output Value (V) (Y=A⊕B)
D_0 (00)	-0.97 ~ 0	-0.008 ~ 1	-0.04 ~ 1	-0.37 ~ 0
D_1 (01)	-0.04 ~ 1	-0.008 ~ 1	-0.97 ~ 0	-0.37 ~ 0
D_2 (10)	-0.04 ~ 1	-0.008 ~ 1	-0.98 ~ 0	-0.37 ~ 0
D_3 (11)	-0.98 ~ 0	-0.008 ~ 1	-0.04 ~ 1	-0.37 ~ 0

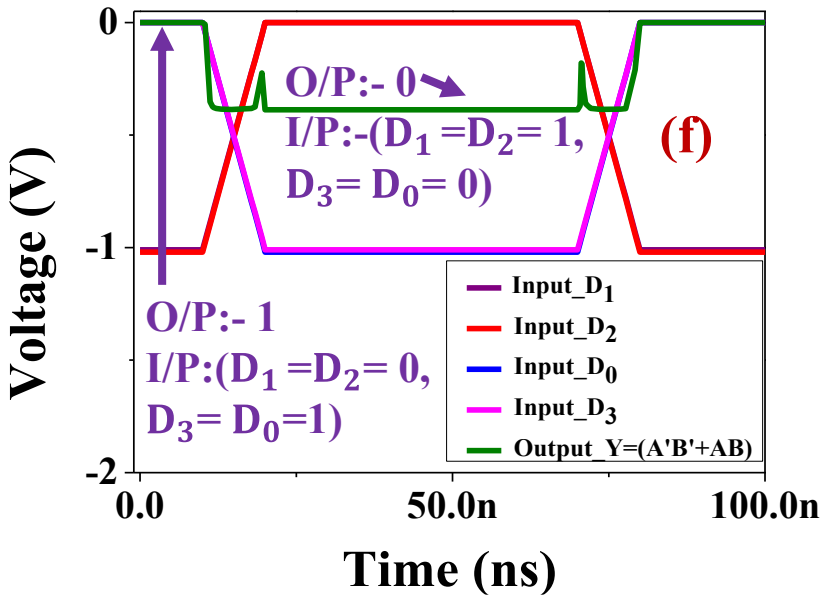


Figure 5.36 (a), (b) Show the implementation of XOR and XNOR logic gates. (c), (d) Present the truth tables of the XOR and XNOR gates, analyzed using the SmartSpice simulator (e), (f) Display the complete circuitry for realizing the XOR and XNOR gates with the help of the 4:1 multiplexer, implemented using the Silvaco Gateway tool.

Table 5.8 Shows Truth Table of "XNOR" Logic Gate

Input	Input Value (V)	Output Value (V) (Y=A⊙B)	Input Value (V)	Output Value (V) (Y=A⊙B)
D_0 (00)	-0.04 ~ 1	-0.008 ~ 1	-0.98 ~ 0	-0.37 ~ 0
D_1 (01)	-0.97 ~ 0	-0.008 ~ 1	-0.04 ~ 1	-0.37 ~ 0
D_2 (10)	-0.98 ~ 0	-0.008 ~ 1	-0.04 ~ 1	-0.37 ~ 0
D_3 (11)	-0.04 ~ 1	-0.008 ~ 1	-0.97 ~ 0	-0.37 ~ 0

5.9 Simulation of Full Adder, Full Subtractor Circuits and Transient Analysis

On successful implementation of Half-Adder circuit using P-TFT in the above section, Hence Full Adder and Full Subtractor circuit is implemented using N-TFT. The diagram of Full Adder circuitry and entire circuitry implemented using "N-TFT" only is shown in **Figure 5.37 (a) and (b).**

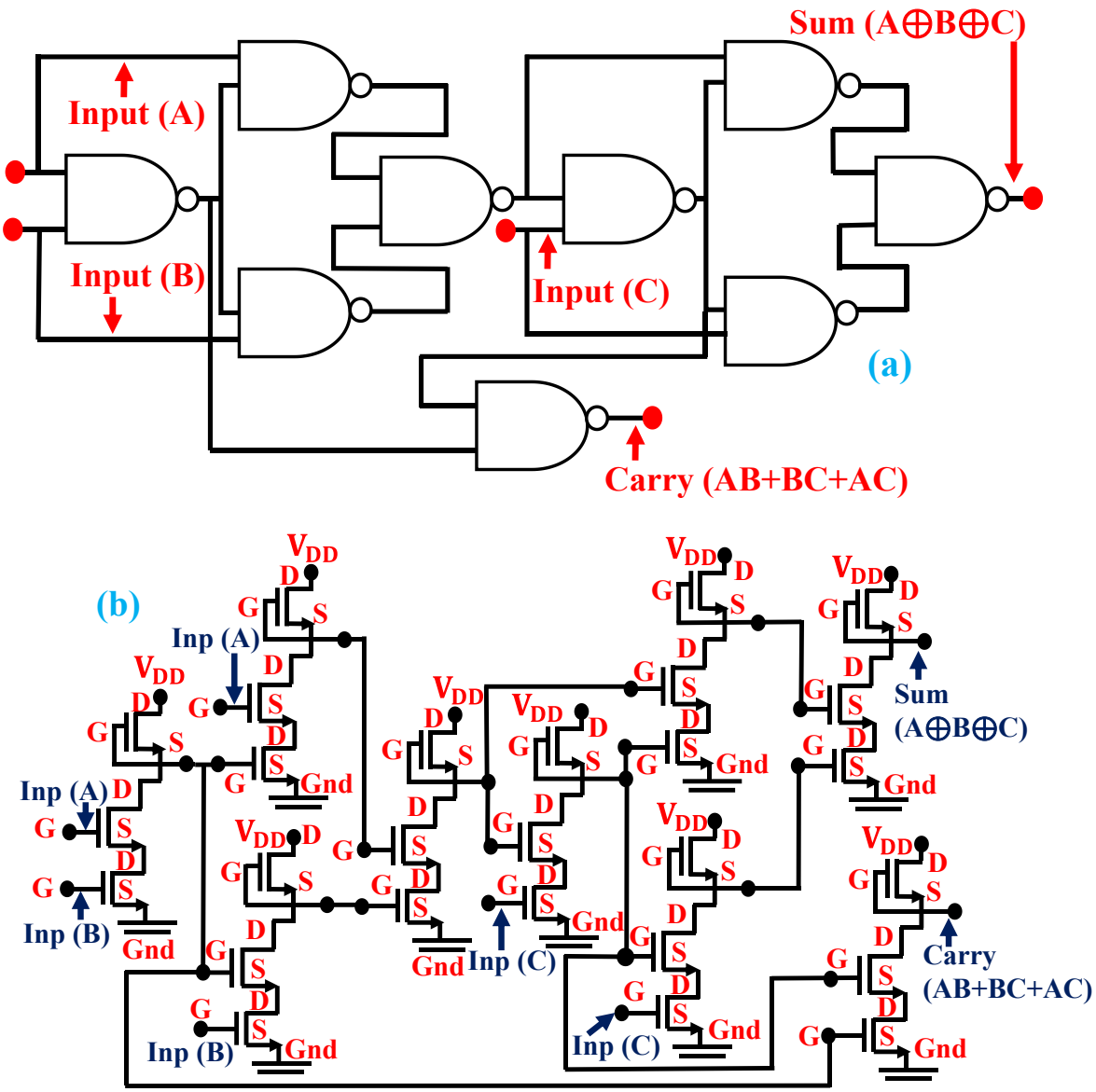
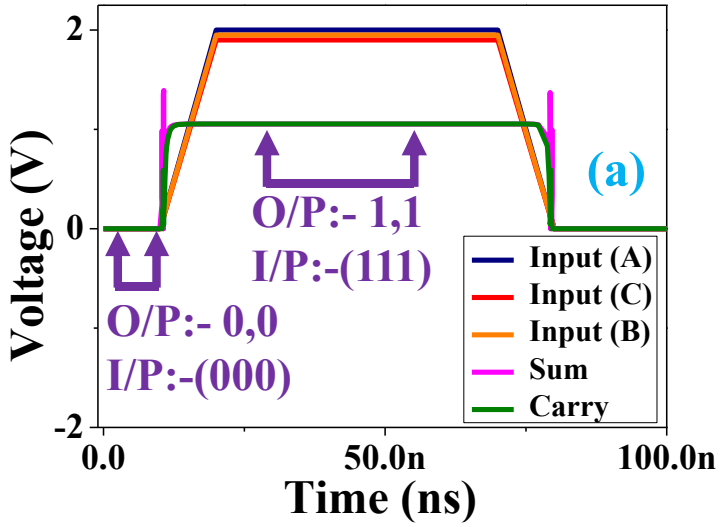
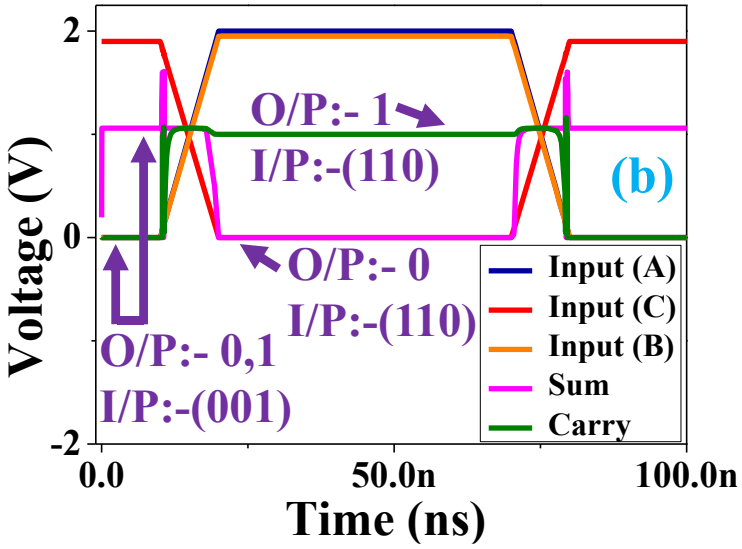
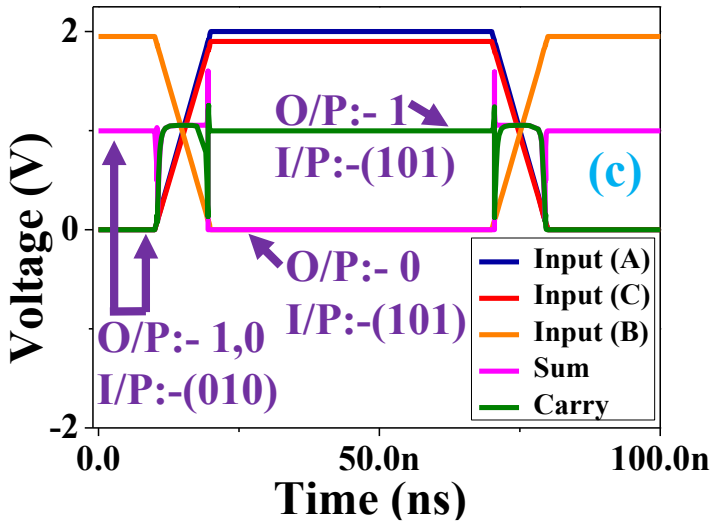


Figure 5.37 (a) Showing the schematic of Full adder circuit (b) Showing the circuitry of Full adder implemented using N-TFT.

In **Figure 5.37 (a)** The full adder circuit is executed using a 2-input NAND gate, where a total nine 2-input NAND gates are utilized for realizing the outputs of the full adder as sum and carry. Where sequence from 000 to 111 are logic inputs for 3 variables A, B and C. Expression of sum and carry in terms of inputs variables are expressed as Sum = A⊕B⊕C and Carry = AB+BC+AC respectively.


2
0
-2
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
(a)
O/P:- 1,1
I/P:-(111)
O/P:- 0,0
I/P:-(000)
Input (A)
Input (C)
Input (B)
Sum
Carry


2
0
-2
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
(b)
O/P:- 1
I/P:-(110)
O/P:- 0
I/P:-(110)
O/P:- 0,1
I/P:-(001)
Input (A)
Input (C)
Input (B)
Sum
Carry


2
0
-2
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
(c)
O/P:- 1
I/P:-(101)
O/P:- 0
I/P:-(101)
O/P:- 1,0
I/P:-(010)
Input (A)
Input (C)
Input (B)
Sum
Carry

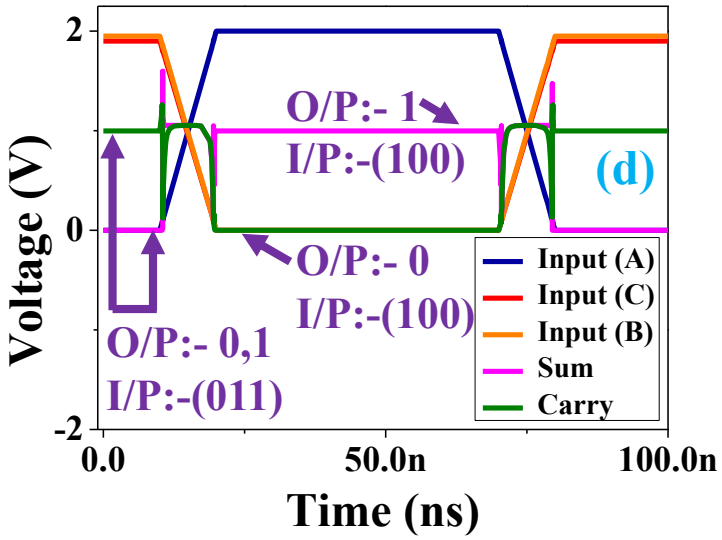
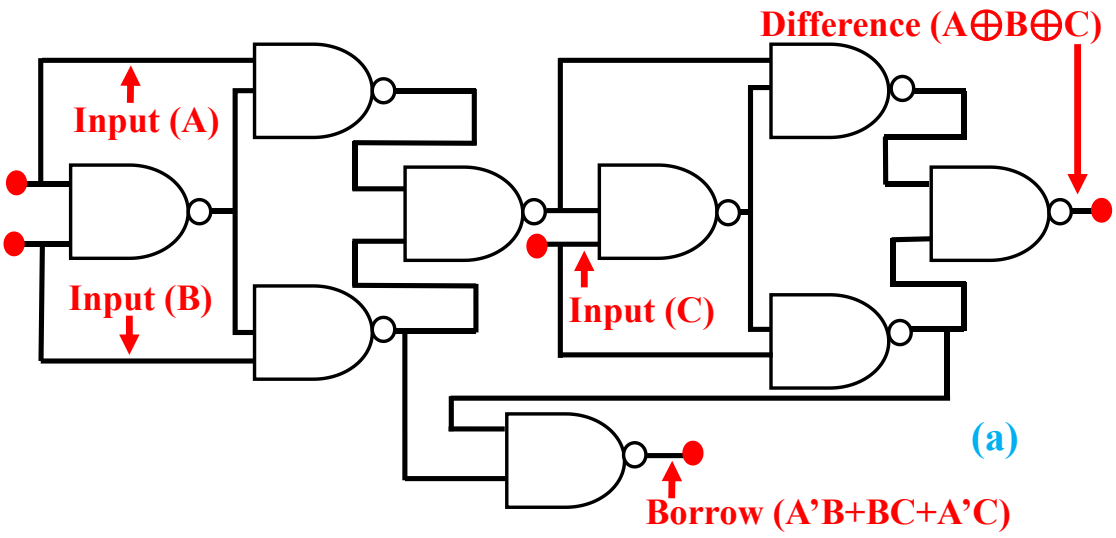


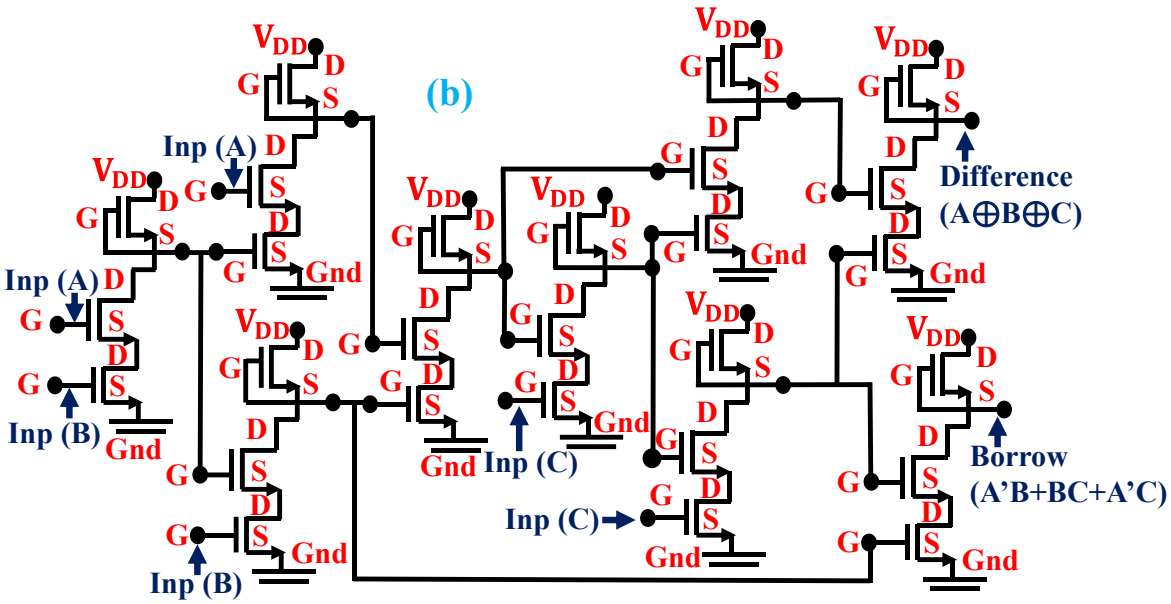
Figure 5.38 (a-d) Indicating the Transient Characteristics of Full Adder Circuit which verify the truth table of full adder for all input from 000 to 111.

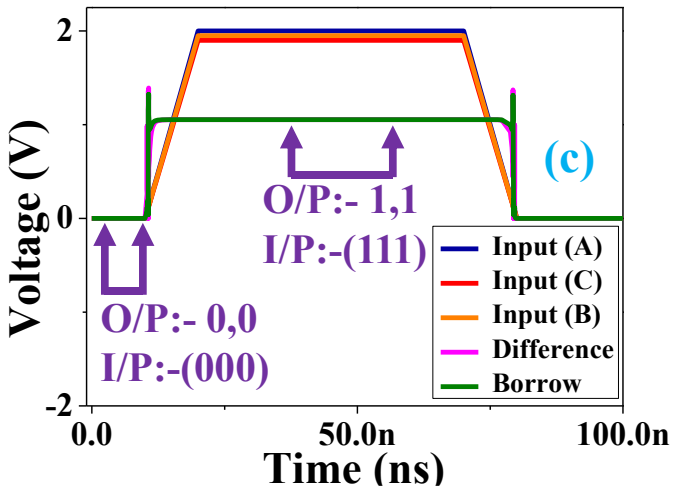
Table 5.9 Truth Table of Full Adder Circuit

S.No.	Input Logic	Output_Sum (V)	Output_Carry (V)
1.	000	2.29E-05 ~ 0	3.00E-06 ~ 0
2.	001	1.06 ~ 1	1.27E-05 ~ 0
3.	010	0.99 ~ 1	2.13E-05 ~ 0
4.	011	2.14E-05 ~ 0	0.997 ~ 1
5.	100	0.997 ~ 1	2.00E-05 ~ 0
6.	101	2.00E-05 ~ 0	0.997 ~ 1
7.	110	2.25E-05 ~ 0	1.00 ~ 1
8.	111	1.054 ~ 1	1.055 ~ 1

Transient analysis is performed with the help of the Smart-Spice Simulator, which exists in the Silvaco-Gateway tool for verification of all 8 cases (000,001,010,011,100,101,110, and 111) for 3 inputs A, B, and C, as mentioned in **Figure 5.38 (a-d)**. In **Table 5.9**, the truth table of the full adder is shown for inputs A, B and C having outputs as Sum and Carry. Expression of sum and carry in terms of inputs variables are expressed as Sum = $A \oplus B \oplus C$ and Carry = AB+BC+AC respectively.


Difference (A⊕B⊕C)
Input (A)
Input (B)
Input (C)
(a)
Borrow (A'B+BC+A'C)


(b)
VDD
Gnd
Inp (A)
Inp (B)
Inp (C)
Difference
(A⊕B⊕C)
Borrow
(A'B+BC+A'C)


(c)
Voltage (V)
Time (ns)
2
0
-2
0.0
50.0n
100.0n
O/P:- 1,1
I/P:-(111)
O/P:- 0,0
I/P:-(000)
Input (A)
Input (C)
Input (B)
Difference
Borrow

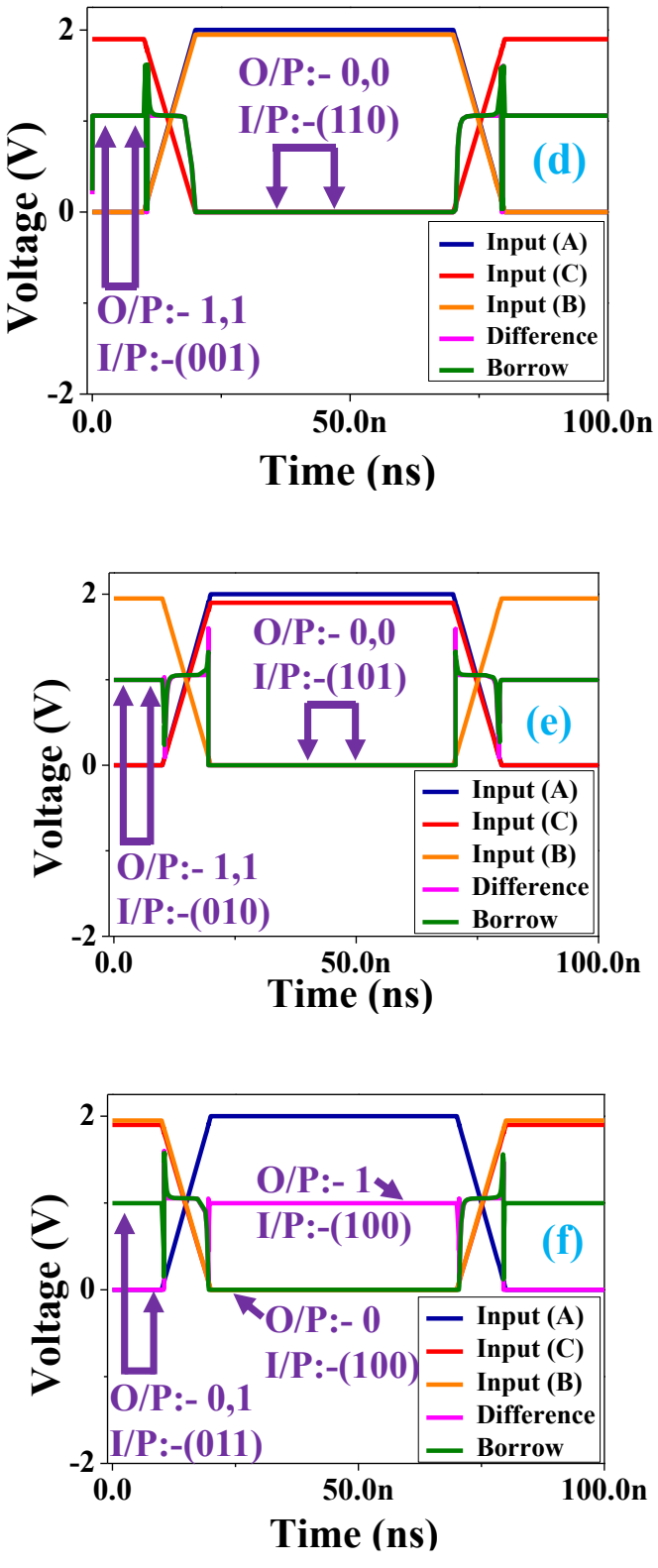


Figure 5.39 (a) Showing the schematic of Full subtractor circuit (b) Showing the circuitry of Full subtractor implemented using N-TFT (c-f) Indicating the truth table of full subtractor for all input from 000 to 111.

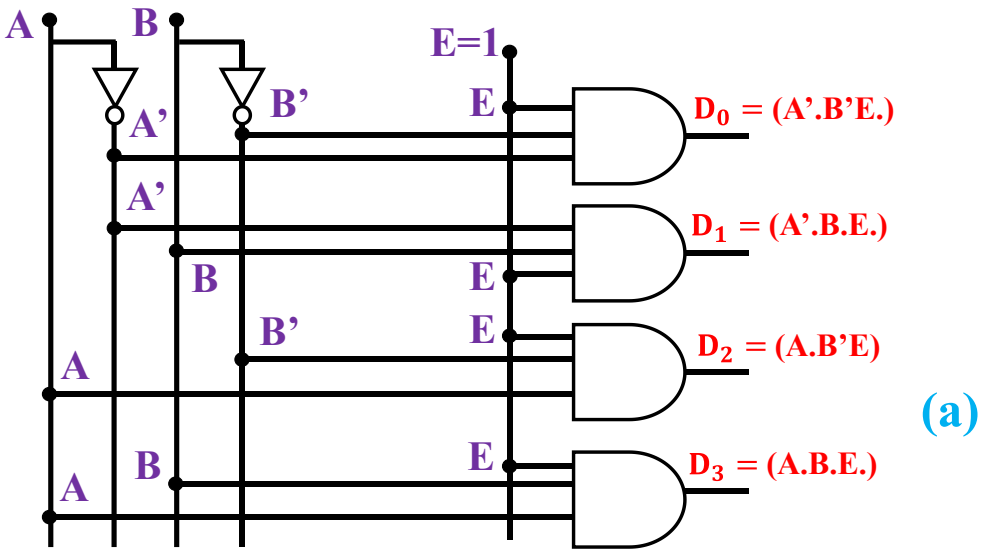
Expression of difference and borrow in terms of inputs variables A, B and C are expressed as Difference = A⊕B⊕C and Borrow =A'B+BC+A'C respectively. In **Figure 5.39 (a)**, a full subtractor circuit is implemented using a 2-input NAND gate. The transient analysis of this full subtractor is done in the same manner as for the full adder using the Smart-Spice Simulator for verifying all cases for the three inputs A, B, and C shown in **Figure 5.39 (c–f)**.

Table 5.10 Truth Table of Full Subtractor Circuit

S.No.	Input Logic	Output Difference (V)	Output Borrow (V)
1.	000	2.29E-05 ~ 0	2.30E-05 ~ 0
2.	001	1.06 ~ 1	1.06 ~ 1
3.	010	0.998 ~ 1	0.998 ~ 1
4.	011	2.14E-05 ~ 0	0.997 ~ 1
5.	100	0.997 ~ 1	1.85E-05 ~ 0
6.	101	2.00E-05 ~ 0	1.99E-05 ~ 1
7.	110	2.25E-05 ~ 0	2.25E-05 ~ 0
8.	111	1.054 ~ 1	1.055 ~ 1

In **Table 5.10**, the truth table of the full subtractor is shown, where difference and borrow are mentioned in all possible cases.

5.10 Simulation of 2:4 and 3:8 Decoder Circuits and Transient Analysis



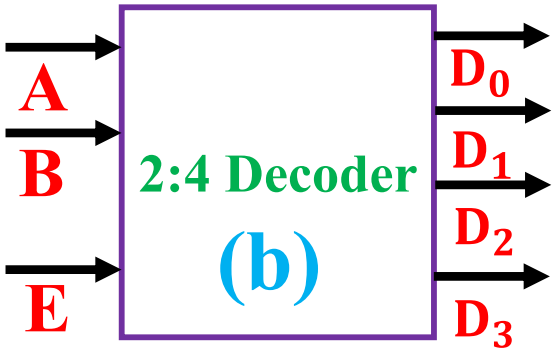
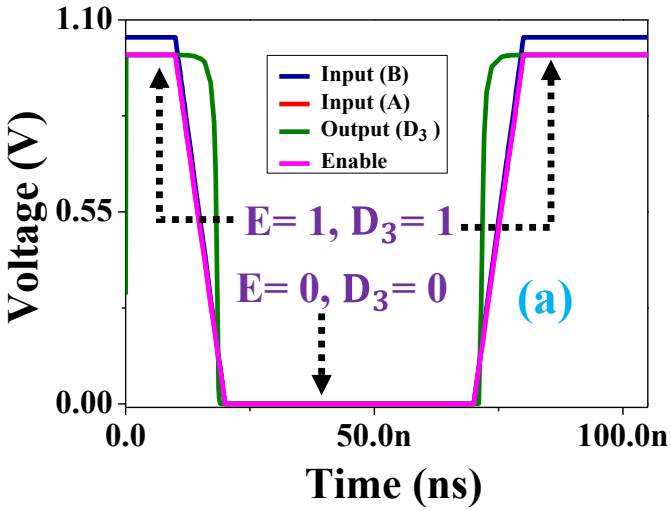
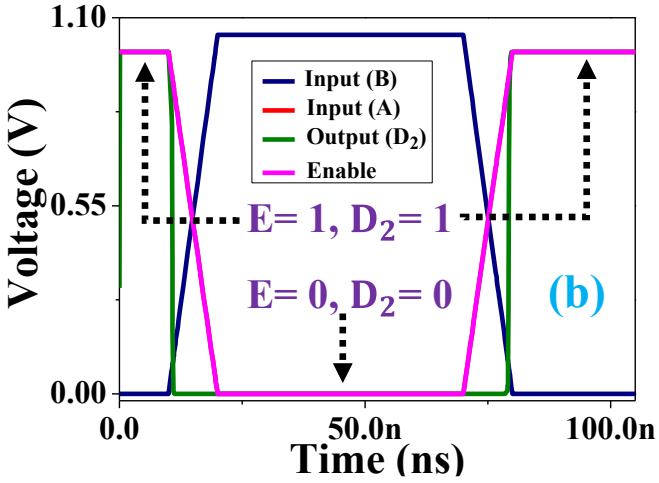


Figure 5.40 (a) , (b) Show the circuit and block diagram of the 2:4 decoder.

The Circuit of 2:4 decoder implemented using logic gates in shown in **Figure 5.40 (a) and (b)**, where inputs 'A' and 'B' serve as the input variables, while 'E' functions as the enable signal. The entire circuitry of 2:4 decoder is realized using “N-TFT” only.





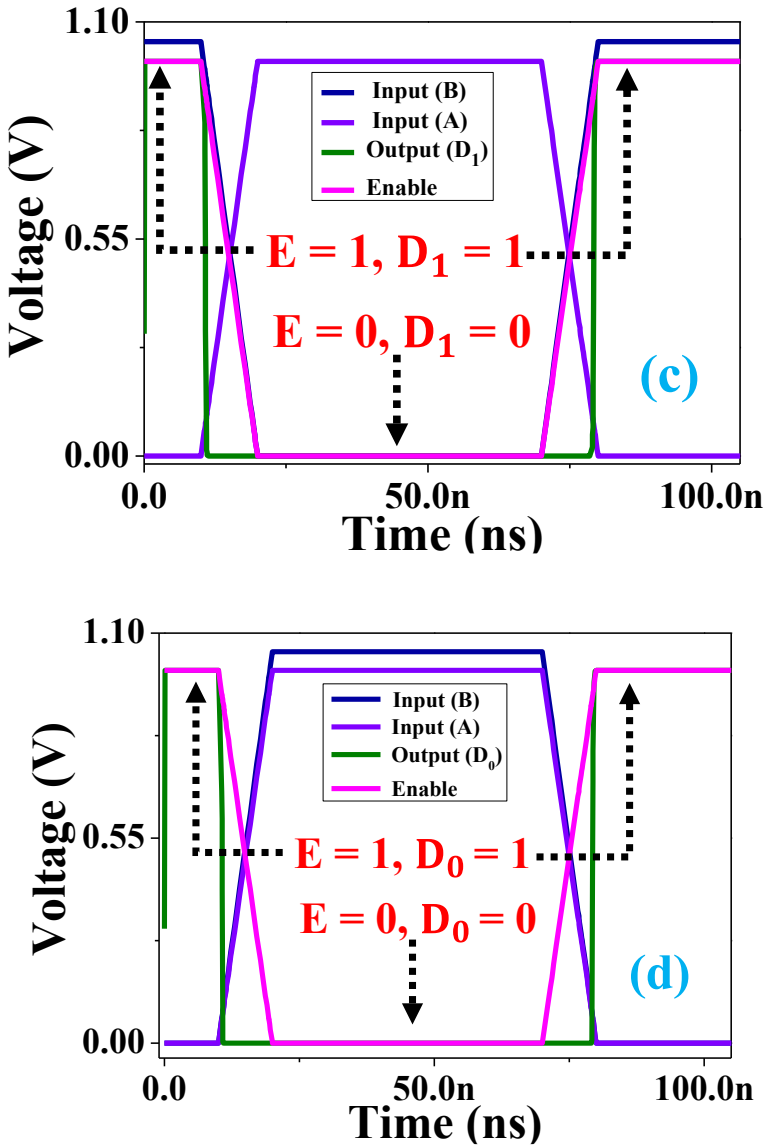


Figure 5.41 (a), (b), (c) and (d) Show truth table of the 2:4 decoder, showing all outputs: D_0, D_1, D_2 and D_3.

Using the Silvaco-Gateway tool, the 2:4 decoder circuit is implemented, as shown in **Figure 5.40 (a).**The inputs 'A,' 'B,' and 'E' are assigned voltage values of 1.0 V, 1.05 V, and 1.0 V, respectively, representing logic '1,' while 0 V indicates logic '0.' Similarly, output voltages of 0 V and 1 V correspond to logic '0' and logic '1,' respectively.

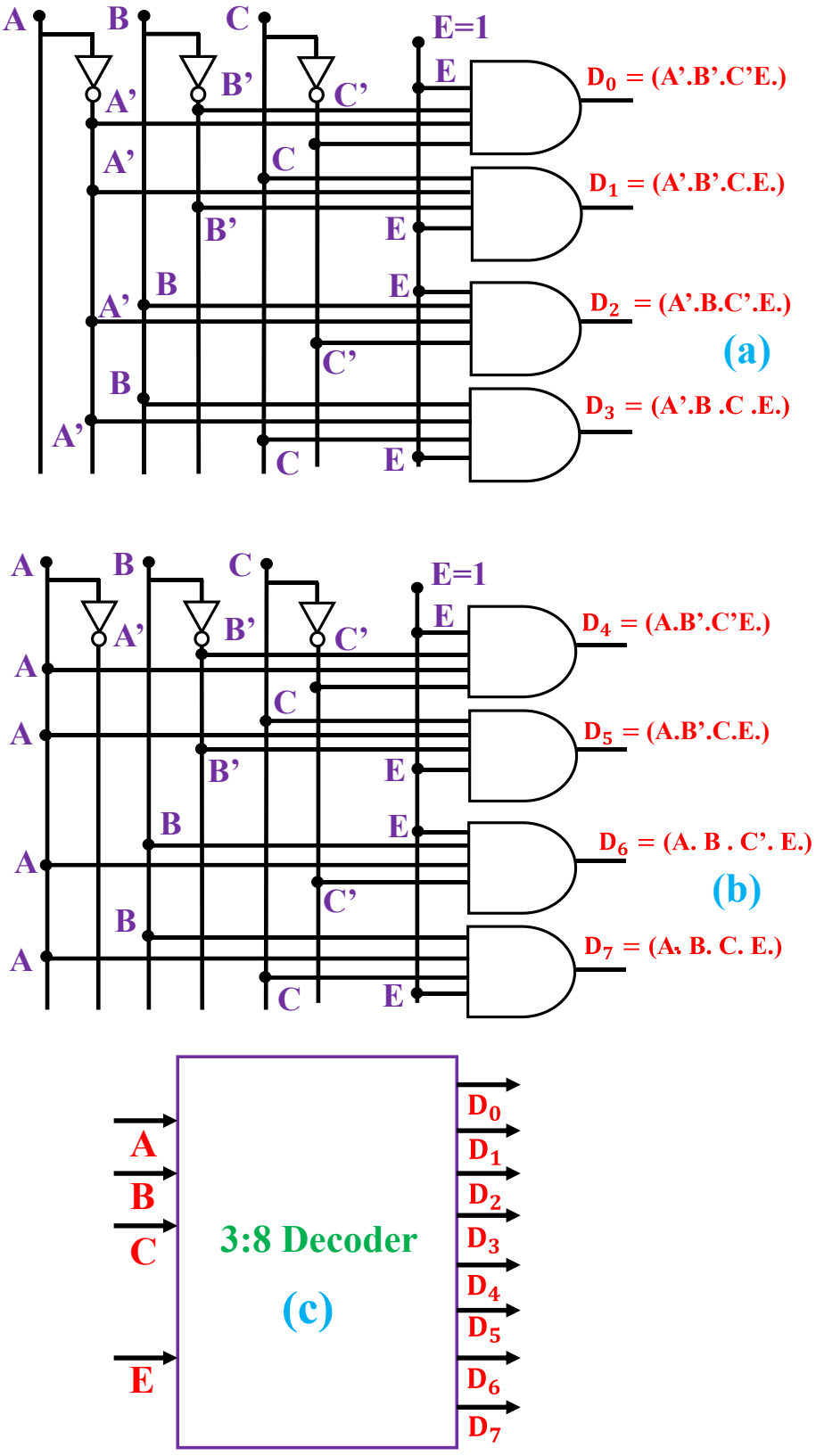
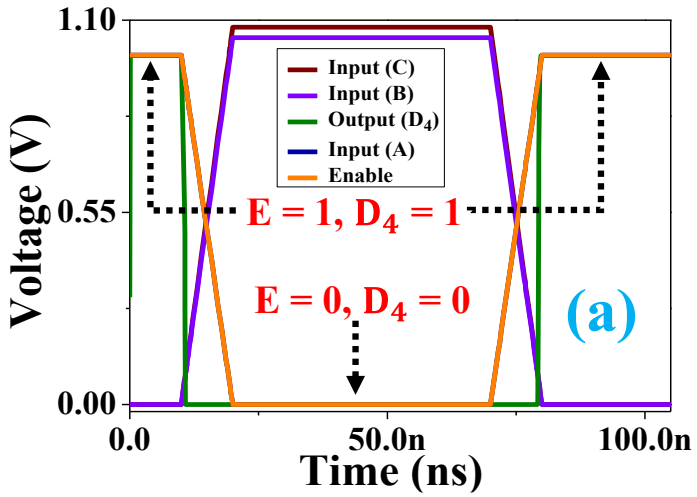


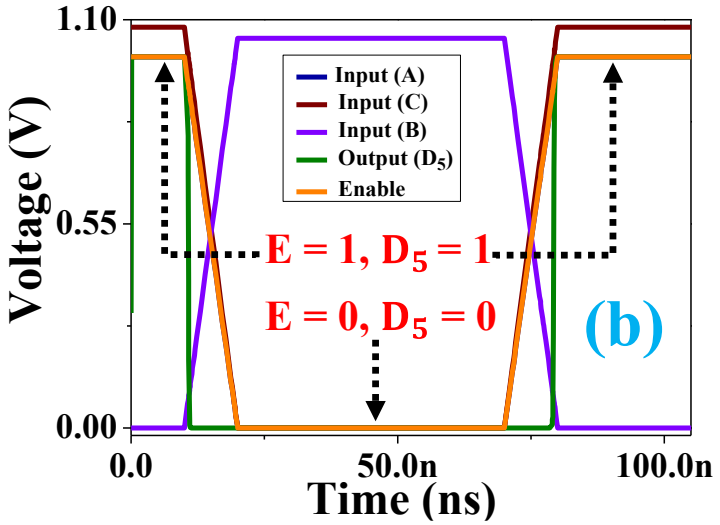
Figure 5.42 (a), (b) illustrate the circuitry of the 3:8 decoder and (c) presents the block diagram of the 3:8 decoder, showing the inputs 'A,' 'B,' and 'C,' along with enable pin 'E'.

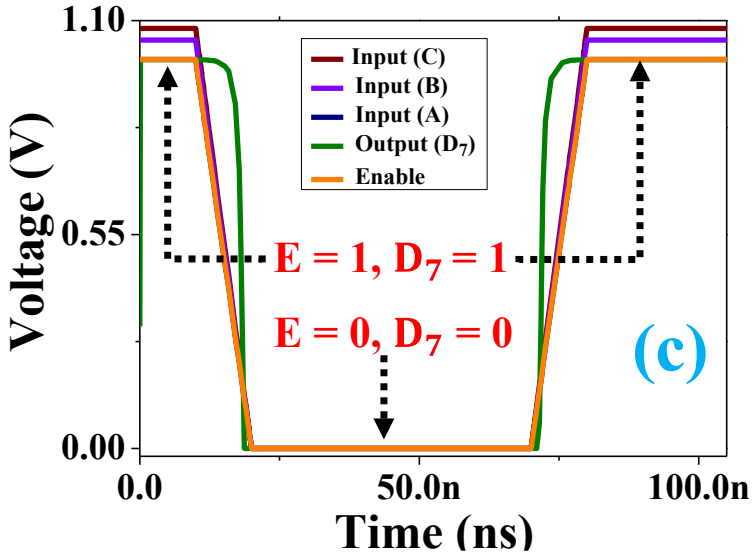
The truth table of the 2:4 decoder circuit, presented in **Table 5.11**, confirms all the input logic combinations.

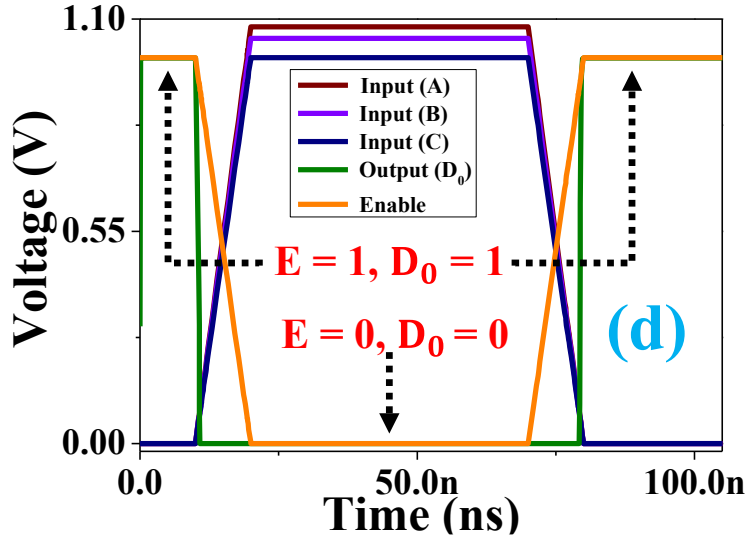
Table 5.11 Truth Table of 2:4 Decoder Circuit

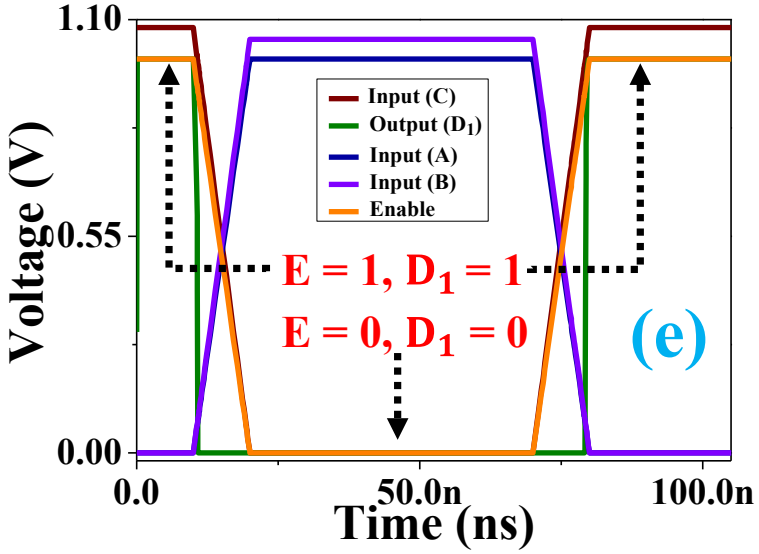
S.No.	Input (E) (V)	Input (A) (V)	Input (B) (V)	Output (V)
1	"0" ~ 0.0	"0" ~ 0.0	"0" ~ 0.0	"0" ~ 0.0
2	"1" ~ 1.0	"0" ~ 0.0	"0" ~ 0.0	"1" ~ 1.0
3	"0" ~ 0.0	"0" ~ 0.0	"1" ~ 1.05	"0" ~ 0.0
4	"1" ~ 1.0	"0" ~ 0.0	"1" ~ 1.05	"1" ~ 1.0
5	"0" ~ 0.0	"1" ~ 1.0	"0" ~ 0.0	"0" ~ 0.0
6	"1" ~ 1.0	"1" ~ 1.0	"0" ~ 0.0	"1" ~ 1.0
7	"0" ~ 0.0	"1" ~ 1.0	"1" ~ 1.05	"0" ~ 0.0
8	"1" ~ 1.0	"1" ~ 1.0	"1" ~ 1.05	"1" ~ 1.0

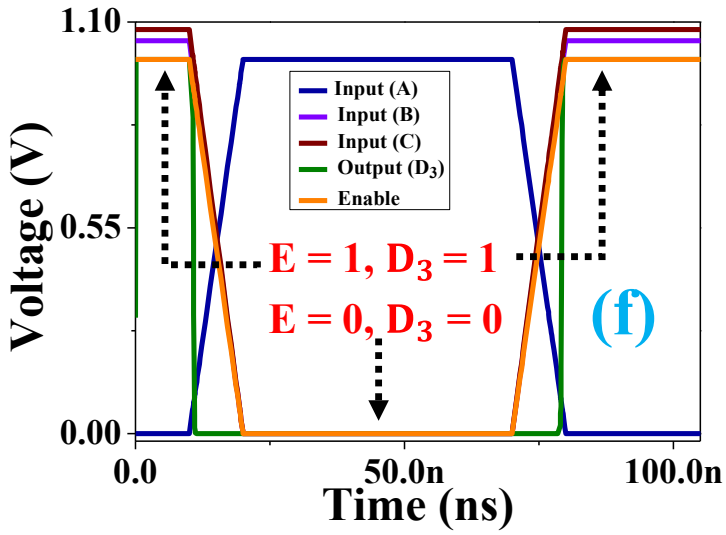


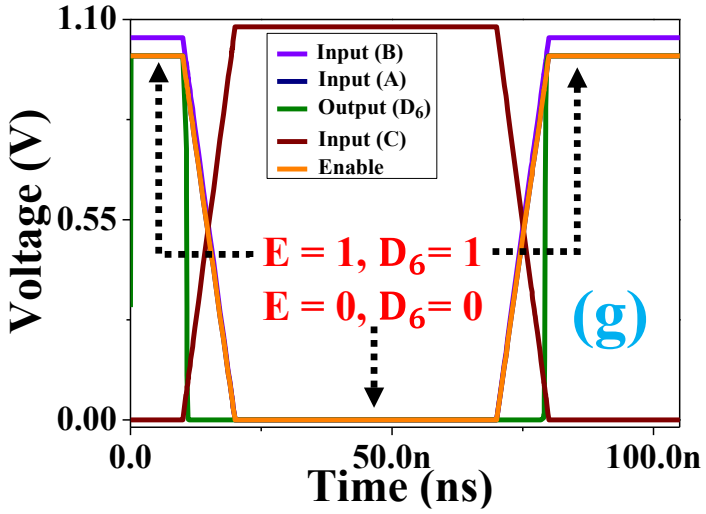



1.10
0.55
0.00
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
Input (C)
Input (B)
Input (A)
Output (D7)
Enable
E = 1, D7 = 1
E = 0, D7 = 0
(c)


1.10
0.55
0.00
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
Input (A)
Input (B)
Input (C)
Output (D0)
Enable
E = 1, D0 = 1
E = 0, D0 = 0
(d)


1.10
0.55
0.00
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
Input (C)
Output (D1)
Input (A)
Input (B)
Enable
E = 1, D1 = 1
E = 0, D1 = 0
(e)





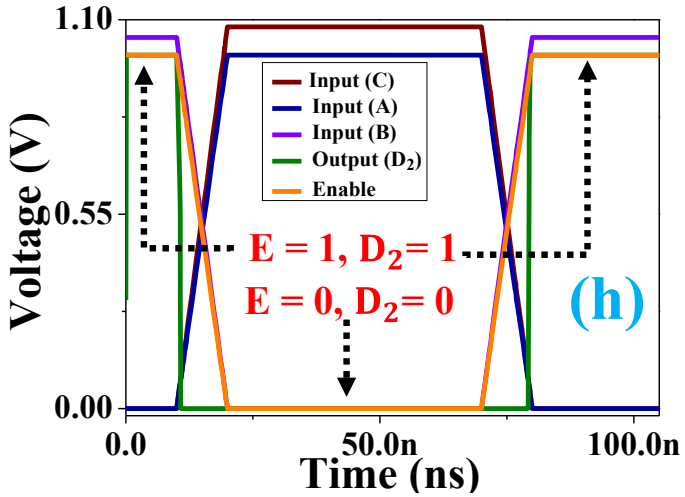


Figure 5.43 (a), (b), (c), (d), (e), (f), (g) and (h) Showing the truth table of the 3:8 decoder, showing all outputs including D_0 to D_7.

Figure 5.42 (a-c) illustrates the 3:8 decoder circuit, while **Figure 5.43 (a-h)** presents the transient analysis for the 3:8 decoder circuit, conducted using a similar methodology as described earlier for the 2:4 decoder circuit in **Figure 5.41 (a-d) and Table 5.12**

Table 5.12 Truth Table of 3:8 Decoder Circuit

S.No.	Input (E) (V)	Input (A) (V)	Input (B) (V)	Input (C) (V)	Output (V)
1	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0
2	“1” ~ 1.0	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.0
3	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.08	“0” ~ 0.0
4	“1” ~ 1.0	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.08	“1” ~ 1.0
5	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.05	“0” ~ 0.0	“0” ~ 0.0
6	“1” ~ 1.0	“0” ~ 0.0	“1” ~ 1.05	“0” ~ 0.0	“1” ~ 1.0
7	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.05	“1” ~ 1.08	“0” ~ 0.0
8	“1” ~ 1.0	“0” ~ 0.0	“1” ~ 1.05	“1” ~ 1.08	“1” ~ 1.0
9	“0” ~ 0.0	“1” ~ 1.0	“0” ~ 0.0	“0” ~ 0.0	“0” ~ 0.0
10	“1” ~ 1.0	“1” ~ 1.0	“0” ~ 0.0	“0” ~ 0.0	“1” ~ 1.0
11	“0” ~ 0.0	“1” ~ 1.0	“0” ~ 0.0	“1” ~ 1.08	“0” ~ 0.0
12	“1” ~ 1.0	“1” ~ 1.0	“0” ~ 0.0	“1” ~ 1.08	“1” ~ 1.0
13	“0” ~ 0.0	“1” ~ 1.0	“1” ~ 1.05	“0” ~ 0.0	“0” ~ 0.0
14	“1” ~ 1.0	“1” ~ 1.0	“1” ~ 1.05	“0” ~ 0.0	“1” ~ 1.0
15	“0” ~ 0.0	“1” ~ 1.0	“1” ~ 1.05	“1” ~ 1.08	“0” ~ 0.0
16	“1” ~ 1.0	“1” ~ 1.0	“1” ~ 1.05	“1” ~ 1.08	“1” ~ 1.0

Inputs 'A,' 'B,' and 'C' serve as the input variables for the 3:8 decoder, with 'E' functioning as the enable signal.The inputs 'A,' 'B,' 'C,' and the enable signal 'E' are assigned voltage values of 1.0 V, 1.05 V, 1.08 V, and 1.0 V, respectively, representing logic '1,' while 0 V indicates logic '0.' Similarly, the output voltages of 0 V and 1 V correspond to logic '0' and logic '1,' respectively. The truth table of the 3:8 decoder circuit is provided and verified in **Table 5.12**.

5.11 Simulation of 1-Bit ALU Circuit and Transient Analysis

In previous reported work, 1-Bit ALU were already developed but they were implemented using CMOS Technology which requires large number of transistors of both n-type and p-type and circuit is realized using Cadence tool where transistor which only exist in

library is used for circuit implementation [249], [250]. Therefore, in this work only "N-TFT" is utilized for the implementation entire 1-Bit ALU circuits and all the associated combination logic circuits.

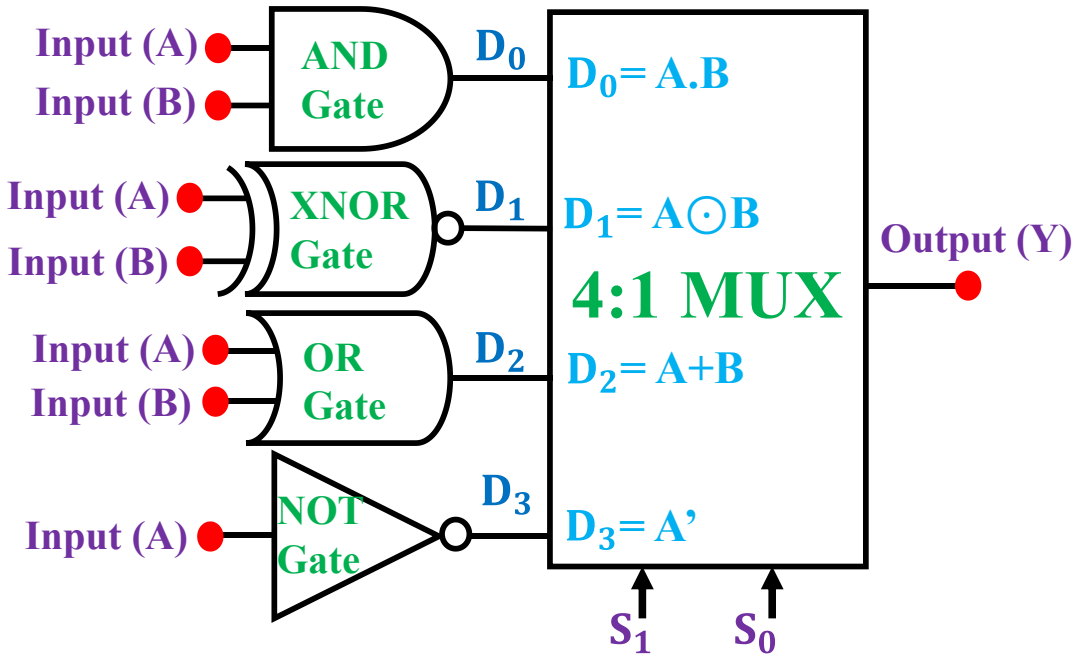


Figure 5.44 Showing the Block Diagram of all the combinational logics of 1-Bit ALU circuit.

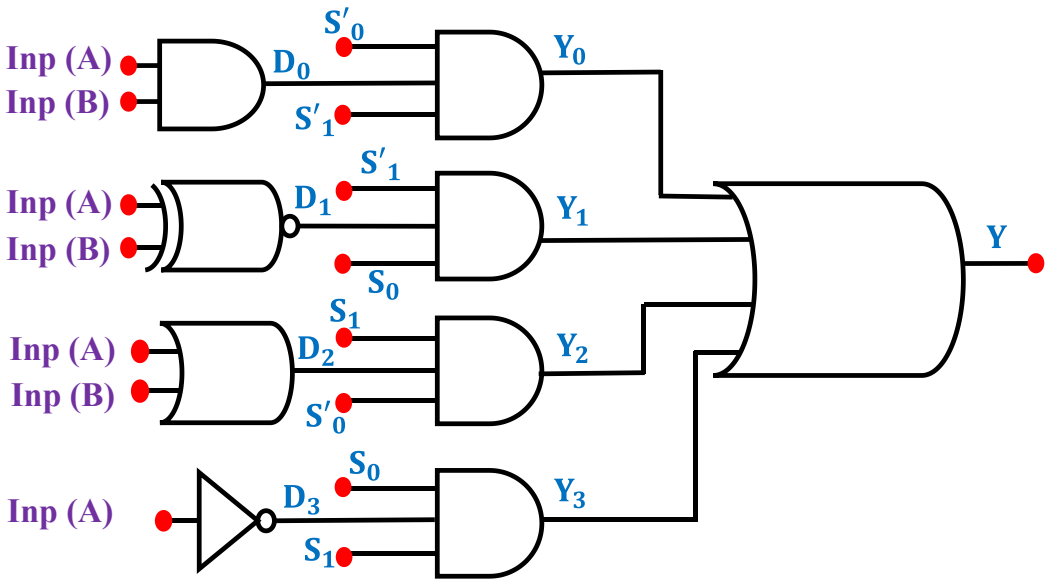


Figure 5.45 Showing the Equivalent Diagram of 1-Bit ALU circuit consisting of "AND", "OR", "NOT" and "XNOR" gates.

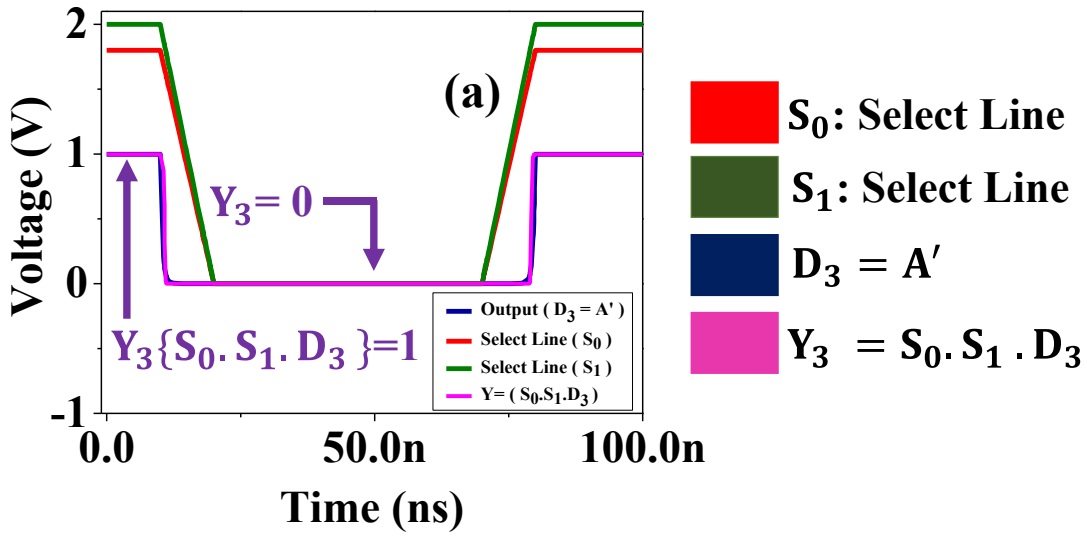
Figure 5.44 shows block diagram of 1 Bit ALU which is implemented using 4:1 Multiplexer. The 4 inputs of 4:1 Multiplexer are 2-inputs "AND", "XNOR", "OR" and "Inverter" gate. **Table 5.13**, states different select lines for opting and performing different ALU operation.

In **Figure 5.45** its equivalent circuit diagram which is made of all the logic gates are mentioned.

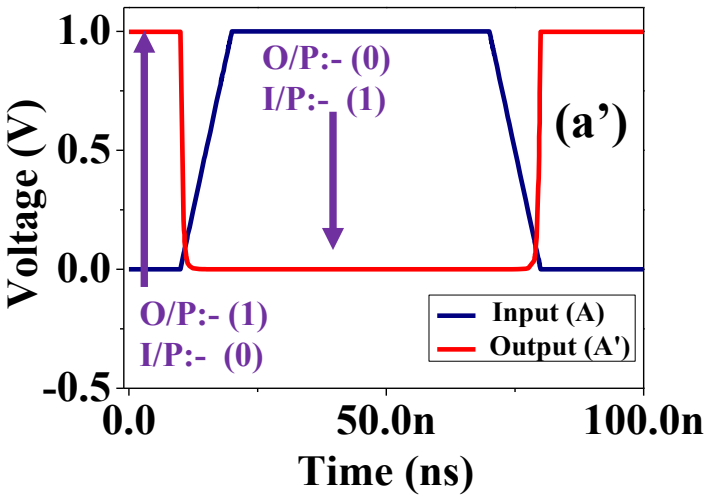
Table 5.13 Explaining different ALU operation according to the select lines logic

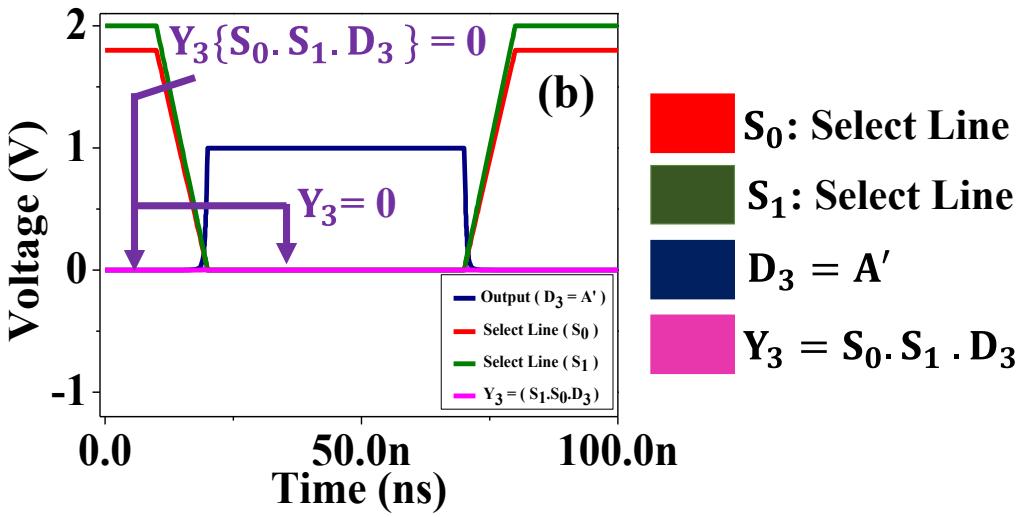
S.No.	Select Line (S_1)	Select Line (S_0)	ALU Operation	ALU Output
1.	0	0	AND	Y=A.B
2.	0	1	XNOR	Y=A⊙B
3.	1	0	OR	Y=A+B
4.	1	1	NOT	Y=A'

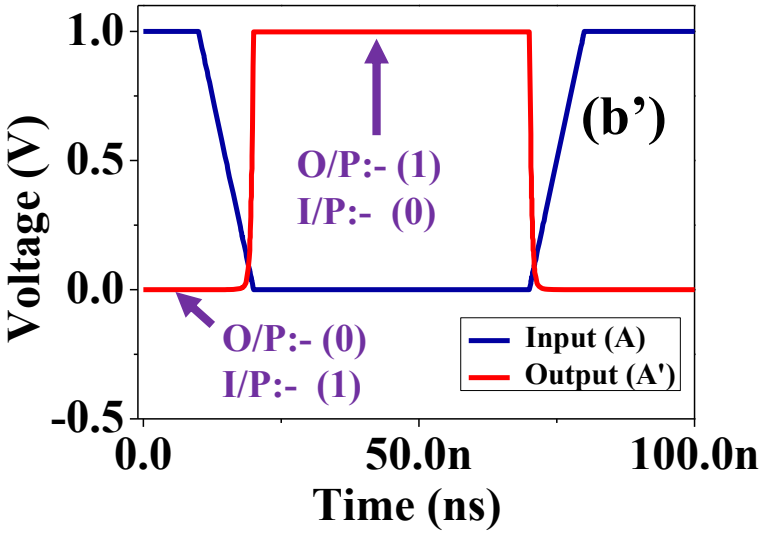
In **Figure 5.45**. Outputs Y_0 , Y_1 , Y_2 and Y_3 are the functions of select lines (S_0 and S_1) and Inputs (A and B). Similarly, Y is the function of (Y_0 - Y_3).

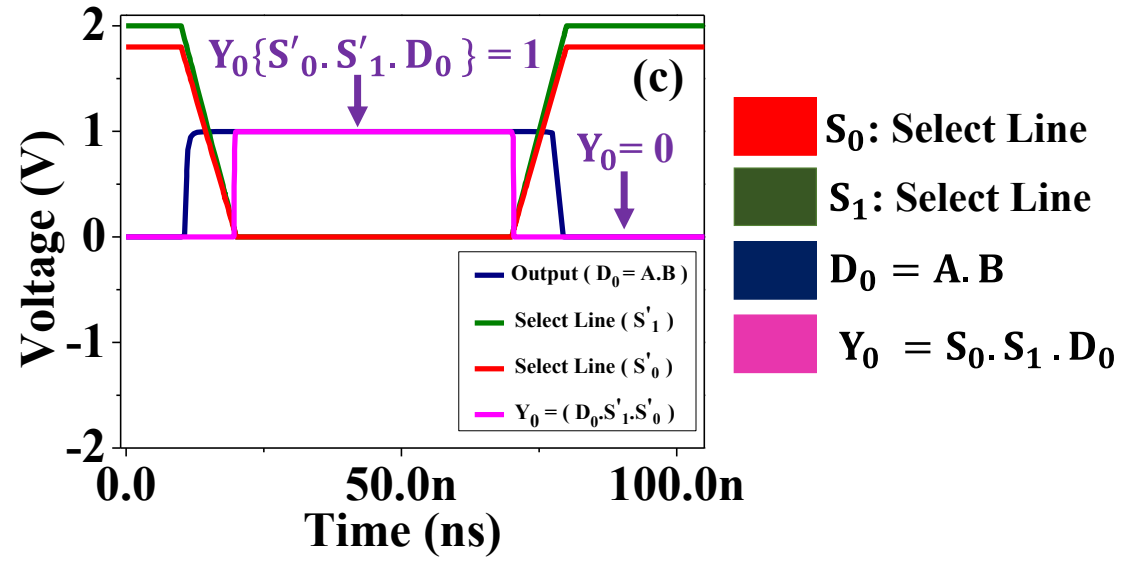


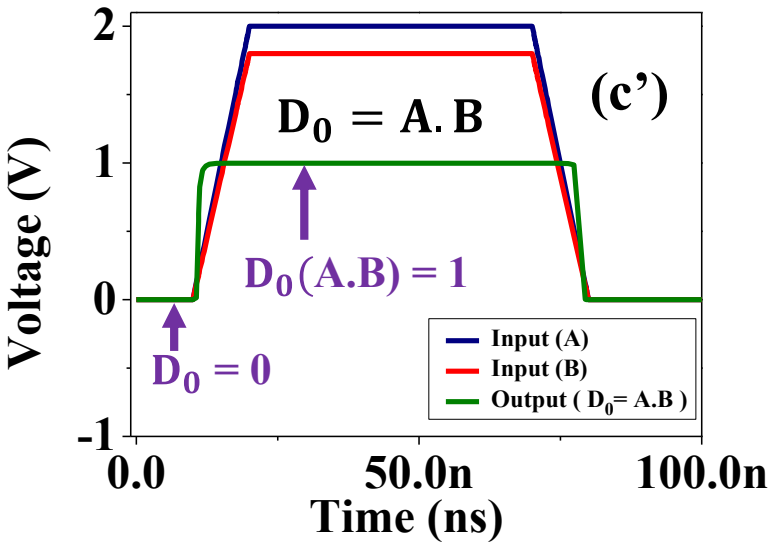
Here, S_0 and S_1 are the select lines and Y_0, Y_1, Y_2, Y_3 are the functions of D_0, D_1, D_2, D_3. In which $D_3 = A'$, $D_2 = (A.B)$, $D_1 = (AB + A'B')$ and $D_0 = (A + B)$

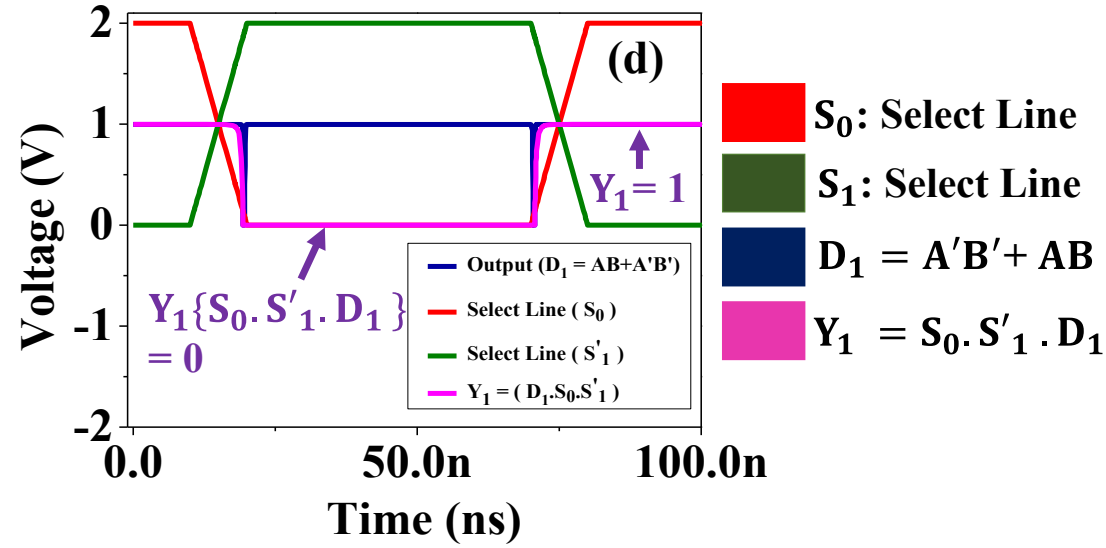

1.0
0.5
0.0
-0.5
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
O/P:- (0)
I/P:- (1)
(a')
O/P:- (1)
I/P:- (0)
Input (A)
Output (A')


2
1
0
-1
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
$Y_3\{S_0.S_1.D_3\} = 0$
(b)
$Y_3 = 0$
Output ($D_3 = A'$)
Select Line (S_0)
Select Line (S_1)
$Y_3 = (S_1.S_0.D_3)$
S_0: Select Line
S_1: Select Line
$D_3 = A'$
$Y_3 = S_0.S_1.D_3$


1.0
0.5
0.0
-0.5
Voltage (V)
0.0
50.0n
100.0n
Time (ns)
O/P:- (1)
I/P:- (0)
(b')
O/P:- (0)
I/P:- (1)
Input (A)
Output (A')


(c)
$Y_0\{S'_0.S'_1.D_0\} = 1$
$Y_0 = 0$
Output (D_0 = A.B)
Select Line (S'_1)
Select Line (S'_0)
Y_0 = (D_0.S'_1.S'_0)
Voltage (V)
Time (ns)
S_0: Select Line
S_1: Select Line
$D_0 = A.B$
$Y_0 = S_0.S_1.D_0$


(c')
$D_0 = A.B$
$D_0(A.B) = 1$
$D_0 = 0$
Input (A)
Input (B)
Output (D_0= A.B)
Voltage (V)
Time (ns)


(d)
$Y_1 = 1$
$Y_1\{S_0.S'_1.D_1\} = 0$
Output (D_1 = AB+A'B')
Select Line (S_0)
Select Line (S'_1)
Y_1 = (D_1.S_0.S'_1)
Voltage (V)
Time (ns)
S_0: Select Line
S_1: Select Line
$D_1 = A'B' + AB$
$Y_1 = S_0.S'_1.D_1$

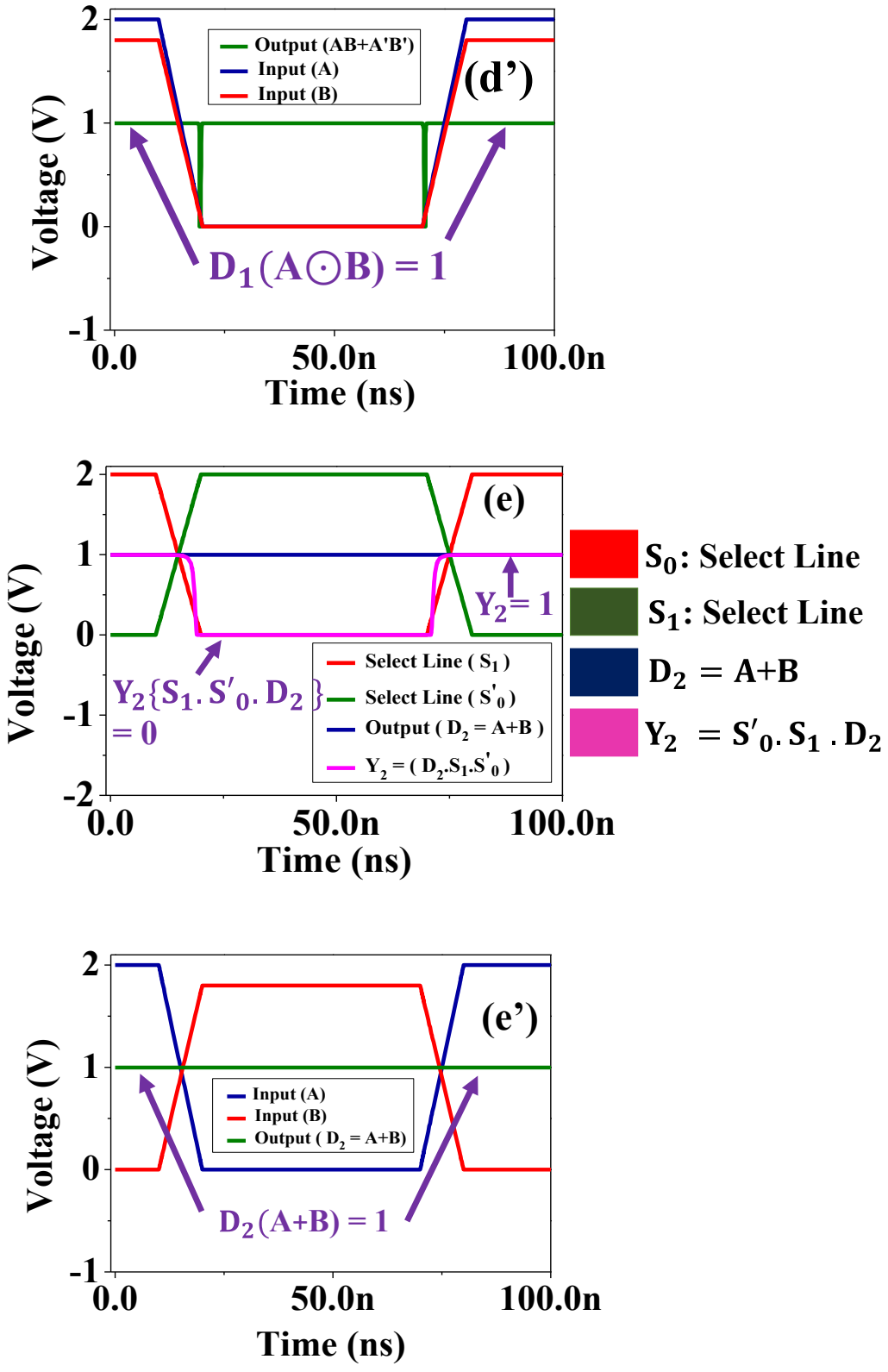


Figure 5.46 (a) and (b) Showing the execution of "NOT" gate operation by ALU when select lines are $S_1 = S_0 = 1$, (a' and b') Indicating the Truth table of "NOT" gate (c)

Showing the execution of "AND" gate operation by ALU when select lines are $S_1 = S_0 = 0$, (c') Indicating the Truth table of "AND" gate (d) Showing the execution of "XNOR" gate operation by ALU when select lines are $S_1 = 0$, $S_0 = 1$, (d') Indicating the Truth table of "XNOR" gate (e) Showing the execution of "OR" gate operation by ALU when select lines are $S_1 = 1$, $S_0 = 0$, (e') Indicating the Truth table of "OR" gate.

With the help of Silvaco-Gateway tool at the initial stage, all the logic gates are implemented and using Smart-Spice simulator which pre-existed in Silvaco-Gateway tool, there corresponding transient analysis is performed to verify the truth table are shown in **Figure 5.46 (a', b', c', d' and e').** As these logic gates are inputs to 4:1 Multiplexer, these 4 inputs (D_0, D_1, D_2 and D_3) are controlled by select lines (S_1 and S_0) according to which desired input is opted and the corresponding ALU operation is performed. Among these 4 inputs of multiplexer only 1 input is active at a time as they governed by select lines and finally the outputs Y_0 , Y_1 , Y_2 and Y_3 are "OR" combination to produce the final output Y. Therefore, according to the logic "0" or "1" of select lines (S_1 and S_0), Y_n n = 0 to 3 would be reflected at the output Y. Y is OR combination of (Y_0 - Y_3) therefore, anyone input logic among (Y_0 - Y_3) tends to "1" would finally lead to output Y to "1" due to "OR" gate property, which is explained in **Table 5.14**.

Table 5.14 Stating different ALU outputs according to the select lines and inputs

S.No.	Select Line (S_1)	Select Line (S_0)	Multiplexer Inputs	ALU Output $Y = (Y_3 + Y_1 + Y_0 + Y_2)$
1.	0	0	$D_0 = 1$ $D_1 = D_2 = D_3 = 0$	$Y = Y_0$, $Y_0 = 1$ $Y_1 = Y_2 = Y_3 = 0$
2.	0	1	$D_1 = 1$ $D_0 = D_2 = D_3 = 0$	$Y_1 = 1$, $Y = Y_1$ $Y_0 = Y_2 = Y_3 = 0$
3.	1	0	$D_2 = 1$ $D_1 = D_0 = D_3 = 0$	$Y_2 = 1$, $Y = Y_2$ $Y_0 = Y_1 = Y_3 = 0$
4.	1	1	$D_3 = 1$ $D_1 = D_2 = D_0 = 0$	$Y_3 = 1$, $Y = Y_3$ $Y_0 = Y_1 = Y_0 = 0$

5.12 Conclusion

In summary, any type of simulated or fabricated device is compact modeled using the Silvaco-Techmodeler tool. Depending upon the nature of the device ("N-TFT/P-TFT"), the same model is opted for to perform compact modeling. After the execution of the modeling process, modeled data is produced, and the accuracy of compact modeling depends upon the mapping between modeled and simulated or fabricated data. This model, which carries all the specifications of a simulated or fabricated device, is further imported into the Silvaco-Gateway tool for the realization of circuits. The level of accuracy evaluated above would be reflected while implementing complex analog circuits, memory circuits, etc. The smart-spice simulator, which is pre-existing at Silvaco-Gateway, is used for DC and transient analysis to check functioning, verify the truth table, and many more. With the help of Silvaco Techmodeler tool, these flexible TFTs were compact modeled and exhibits excellent accuracy ~ 100% with small fraction of error less than 1% (0.41% , 0.94%) for a-IGZO TFT and (0.37% and 0.74%) for PBTTT-C14 based TFT and subsequently employed in the Silvaco Gateway tool for the realization of circuits as basic logic gate families, CMOS inverter circuit, 1-Bit Magnitude Comparator, Half Adder, Full Adder and Subtractor, 1-Bit ALU, 4:1 Multiplexer and 2:4 and 3:8 Decoder circuits.Using Smart-Spice simulator exist in Silvaco-Gateway tool, transient and DC analysis has been also performed for estimating propagation delay, logic swing, etc. and for the verification of truth table for digital circuit. The truth table of all the circuit mentioned above are verified using transient analysis. In the near future using these compact modeled device complex analog and digital circuits, memory circuits , microprocessors, etc. would be realized.

Chapter 6

Stability Analysis of Transparent Low-Power TFT: Impact of Design and Biasing

6.1 Introduction

In previous years, a-IGZO (amorphous indium gallium zinc oxide) has been highly preferred by many researchers as they exhibit features such as a higher magnitude of mobility > 10, enhanced on-off ratio and uniformity, and a wide band gap ~ 3.25 eV, which led to high transparency in the visible region (400-700 nm) [99], [184], [251]–[255]. These features proved fruitful for various applications such as flexible electronics, transparent electronics, AMOLED displays, etc. [255]–[257]. The application of AMOLED display is governed by a important component which is the electrical stability of a-IGZO-based TFT. Similarly, the brightness in the active-matrix display/sensors is controlled by the hysteresis phenomenon in which the drain current of transfer characteristics is varied in forward and reverse directions. Charge injection and charge trapping are some mechanisms that are some causes for hysteresis [255]–[260]. In addition to this, there are some instabilities that arise from electrical stress, such as negative/positive bias stress (NBS/PBS) and negative/positive bias temperature stress (NBTS/PBTS), that alter device characteristics of a-IGZO TFT [260]–[263]. Even the flat panel display is controlled by the positive and negative bias of TFT [264]. Reasons for PBS instability are electrons trapping in the gate dielectric and defects formation in the active layer [260]. In the previously reported work, there are various factors mentioned that led to a shift, such as variation in the magnitude of defect states as donor and acceptor states, oxygen-related defect states, charge transport in dielectric, injection and trapping of mobile charge carriers, slow polarization, ion migration, etc. [263], [263], [265]–[270]. In addition, to overcome power consumption limitations, high-k dielectric materials such

as zirconium oxide (ZrO_2), hafnium oxide (HfO_2), etc., used as gate dielectrics of TFTs as they possess a k value greater than 15, which led to an operating voltage of ~ (1-2 V) [59], [95], [99]. Hence, in this work, using the Silvaco-Atlas tool, a fully transparent a-IGZO-based TFT has been simulated, as device fabrication at the early stage is full of risk and costly in nature. In the previously reported work, positive bias stress analysis has been done, but the device operated at high voltages of ~10, 15, and 20 V [260], [271], [272]. In this simulation, factors such as variable active layer thickness, dielectric layer thickness, and fixed charge density have been done for estimating the stability analysis for this a-IGZO-based TFT.

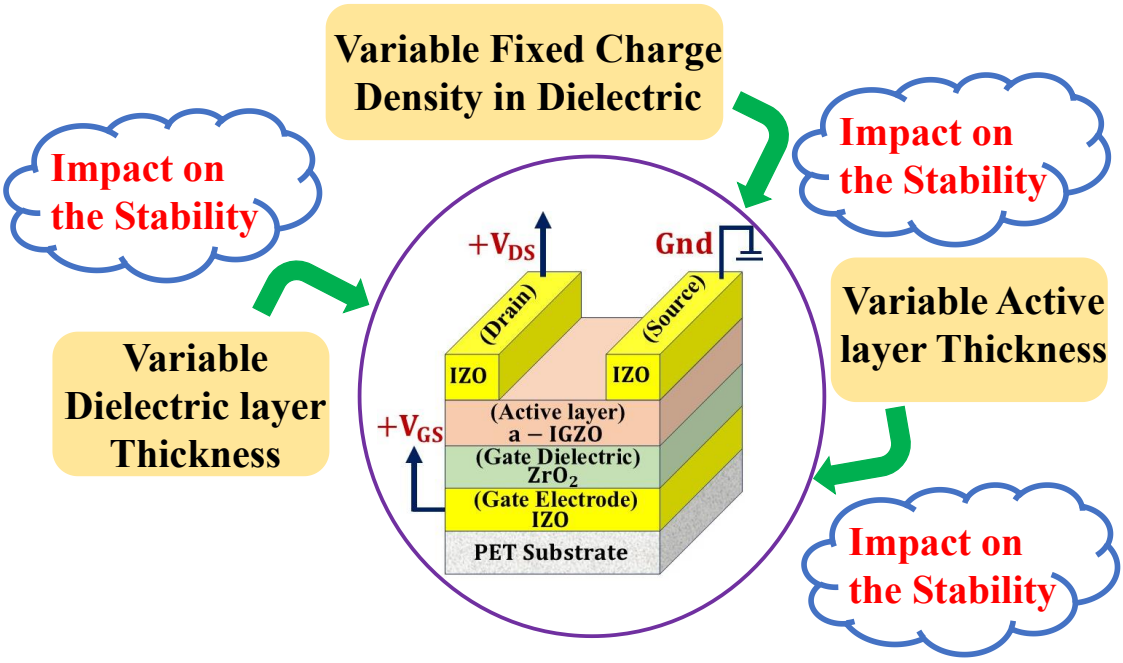


Figure 6.1 Displays the factors that effect on the stability of TFT.

In **Figure 6.2**, a-IGZO (amorphous IGZO) acts as the active layer, ZrO_2 serves as the gate electrode, and IZO (indium zinc oxide) is used as electrodes for the gate, source, and drain. This TFT is simulated over PET substrate to develop a flexible device. The active layer and dielectric layer thickness is varying from 10nm to 30nm and 70 nm to 40 nm; fixed charge density varies from $\pm 1 \times 10^{12}$, and $\pm 5 \times 10^{12}$ cm^{-2}, and to observe the

impact on the hysteresis curve for V_{GS}, it first increases from 0 to 1.5 V, which shows 'Off to On State,' and then decreases from 1.5 to 0 V, which shows 'On to Off State,' respectively.

6.2 Device Structure and Specifications

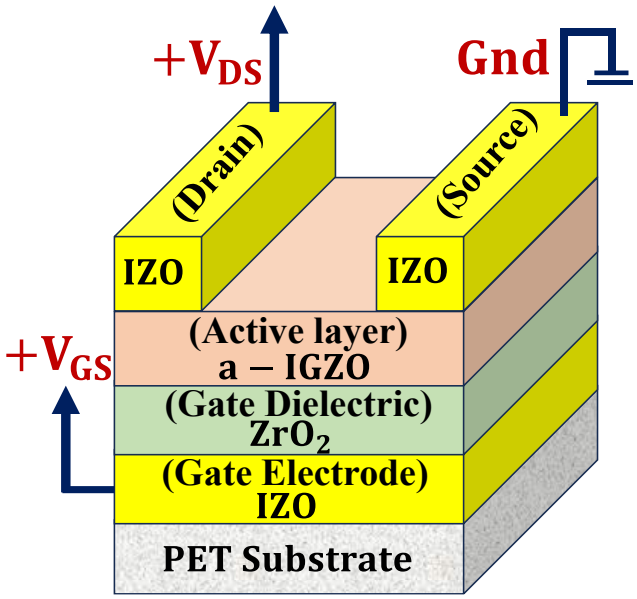


Figure 6.2 Displays the TFT structure in which different materials are utilized as active layer, gate dielectric and electrodes.

6.3 Results and Discussions

The Characteristics curve mentioned in **Figure 6.3. (a-a') and (b)** approve that this device has operating voltage of 1.5 V and the magnitude of saturation current is estimated as 21.3 µA at V_{GS} = 1.5 V. The operation regions of the device are:

1. Linear region and 2. Saturation region.

Condition for linear and Saturation are as follows in equation (6.1) and (6.2) respectively:

$$V_{DS} < V_{GS} - V_{TH} \qquad (6.1)$$

$$V_{DS} \geq V_{GS} - V_{TH} \qquad (6.2)$$

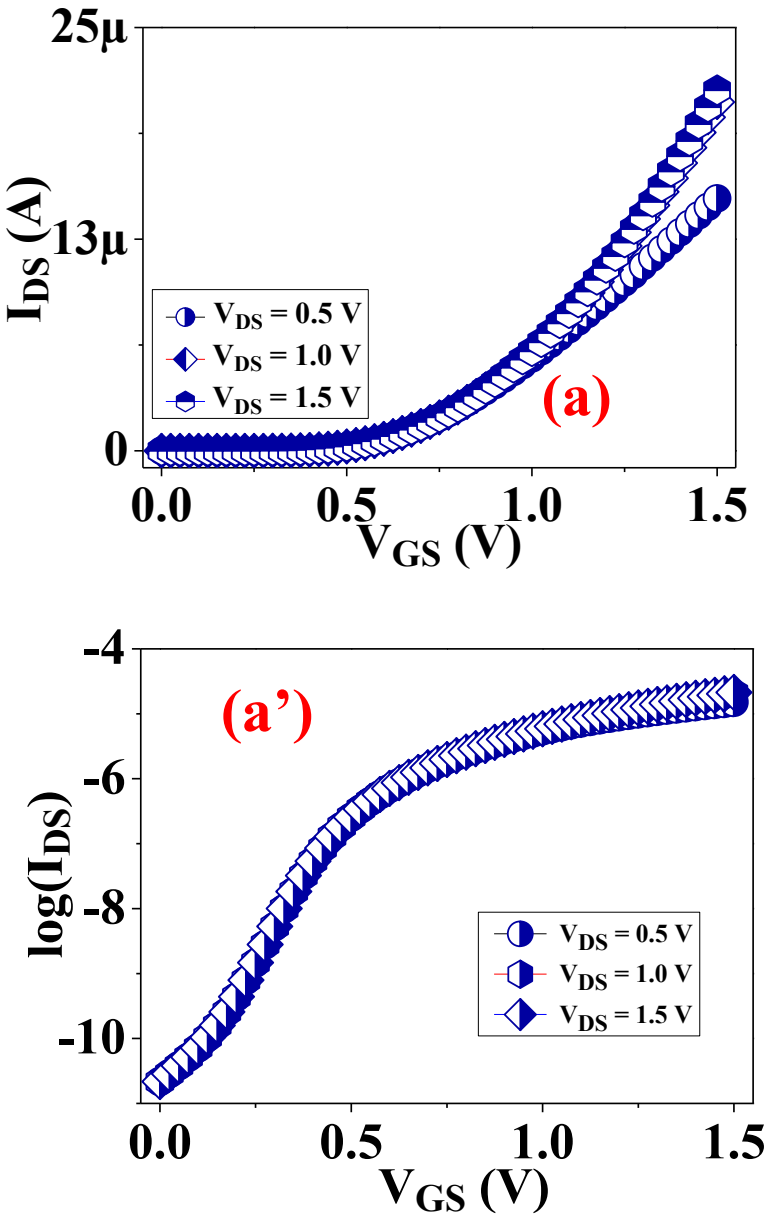
To estimate the performance parameters of the device, the region of operation of device

should be in saturation region.

In saturation region, drain current equation is stated as:

$$I_{DS} = \mu_n \frac{W}{2L} C_{OX}(V_{GS} - V_{TH})^2 \qquad (6.3)$$

Where μ_n is electron-mobility, C_{OX} is oxide capacitance, W and L are channel width and length. V_{DS} is drain-source voltage, V_{GS} is gate-source voltage and V_{TH} is threshold voltage. The width (W) and length (L) of this device are taken as 180 μm and 30 μm .



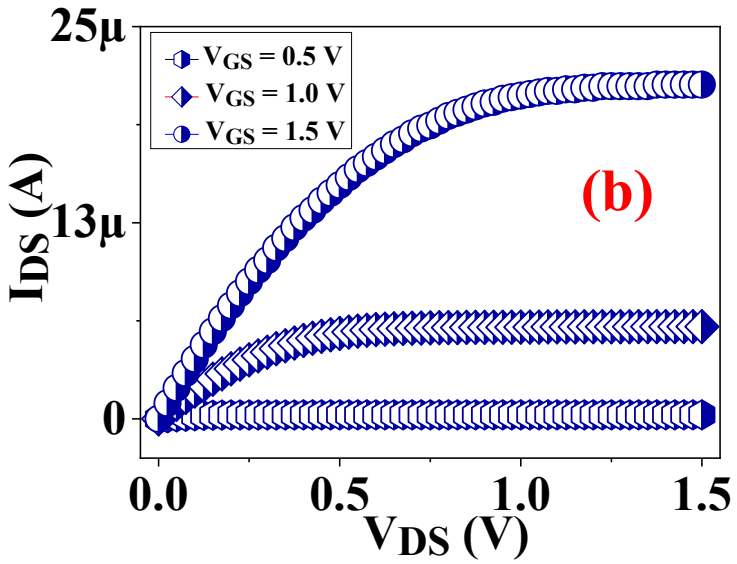


Figure 6.3 (a) States the Transfer characteristics curve ($I_{DS} - V_{GS}$) curve for V_{DS} changes from 0 to 1.5 V with an increase of 0.5 V (a') logarithmic scale of transfer curve (b) States the Output characteristics curve ($I_{DS} - V_{DS}$) curve for V_{GS} changes from 0 to 1.5 V with an increase of 0.5 V.

The performance parameters of the simulated device are evaluated as $I_{ON}/I_{OFF} \sim 10^6$, $\mu_n \sim 8.37\ {}^{cm^2}/_{Vs}$, V_{TH} = 0.21 V and $SS = 84\ {}^{mV}/_{decade}$.

6.4 Hysteresis Curve Analysis

A. Variation in Dielectric layer Thickness

The dielectric layer thickness ($T_{dielectric}$) also impacts the variation in V_{TH} [270], [273]. To examine the behavior of the hysteresis curve in which the change in threshold voltage (ΔV_{TH}) is calculated for the device for both cases, "Off to On State" and vice-versa. In this case, the alteration in the thickness of the dielectric layer (70/60/50/40 nm) is performed to analyze (ΔV_{TH}) on different thicknesses, which has been shown in **Figures. 6.4 to 6.7**.

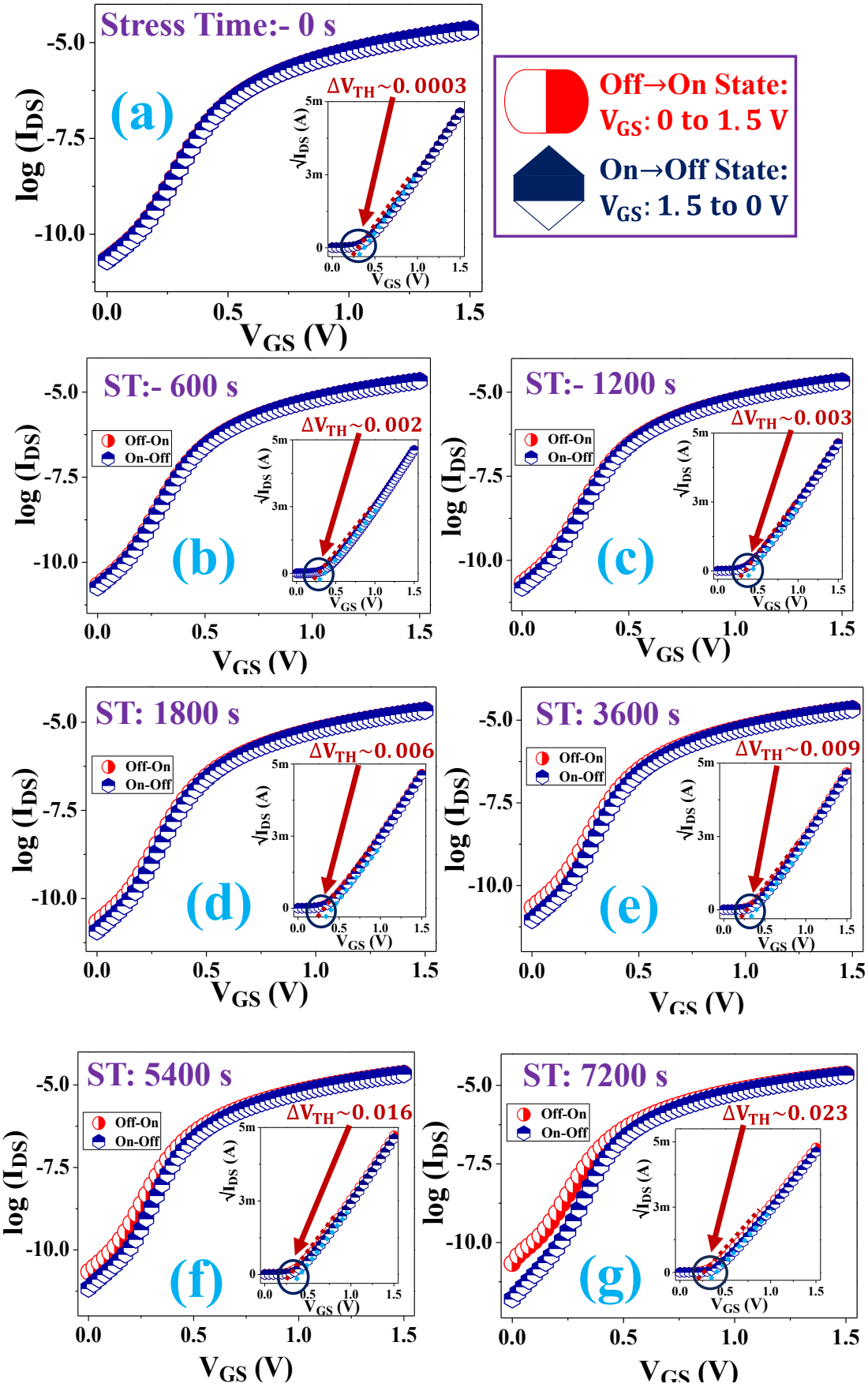


Figure 6.4 (a)-(g) Displays the transfer characteristics for different stress time, when

active layer thickness and dielectric thickness are taken as 30 nm and 40 nm.

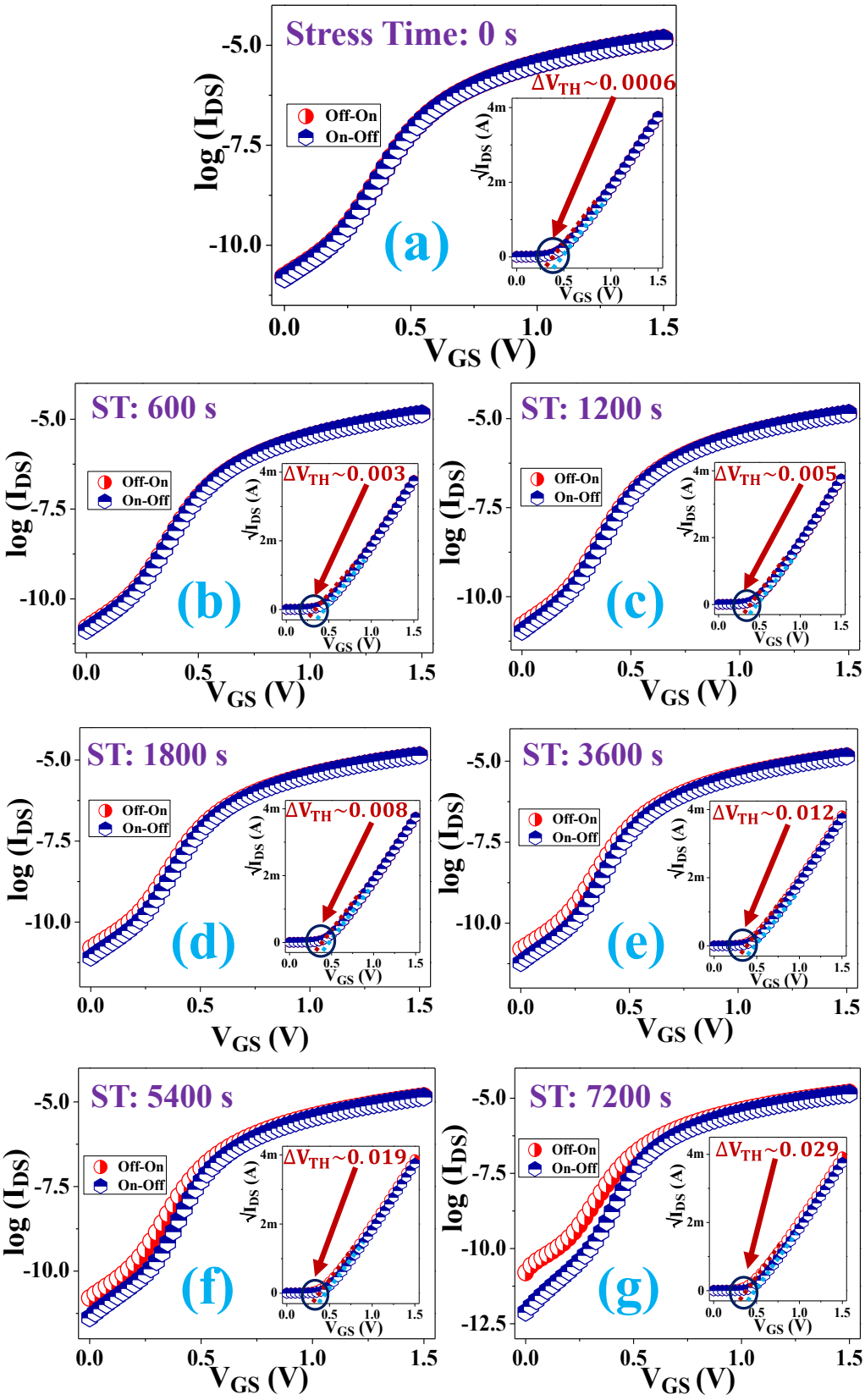


Figure 6.5 (a)-(g) Displays the transfer characteristics for different stress time, when

active layer thickness and dielectric thickness are taken as 30 nm and 50 nm.

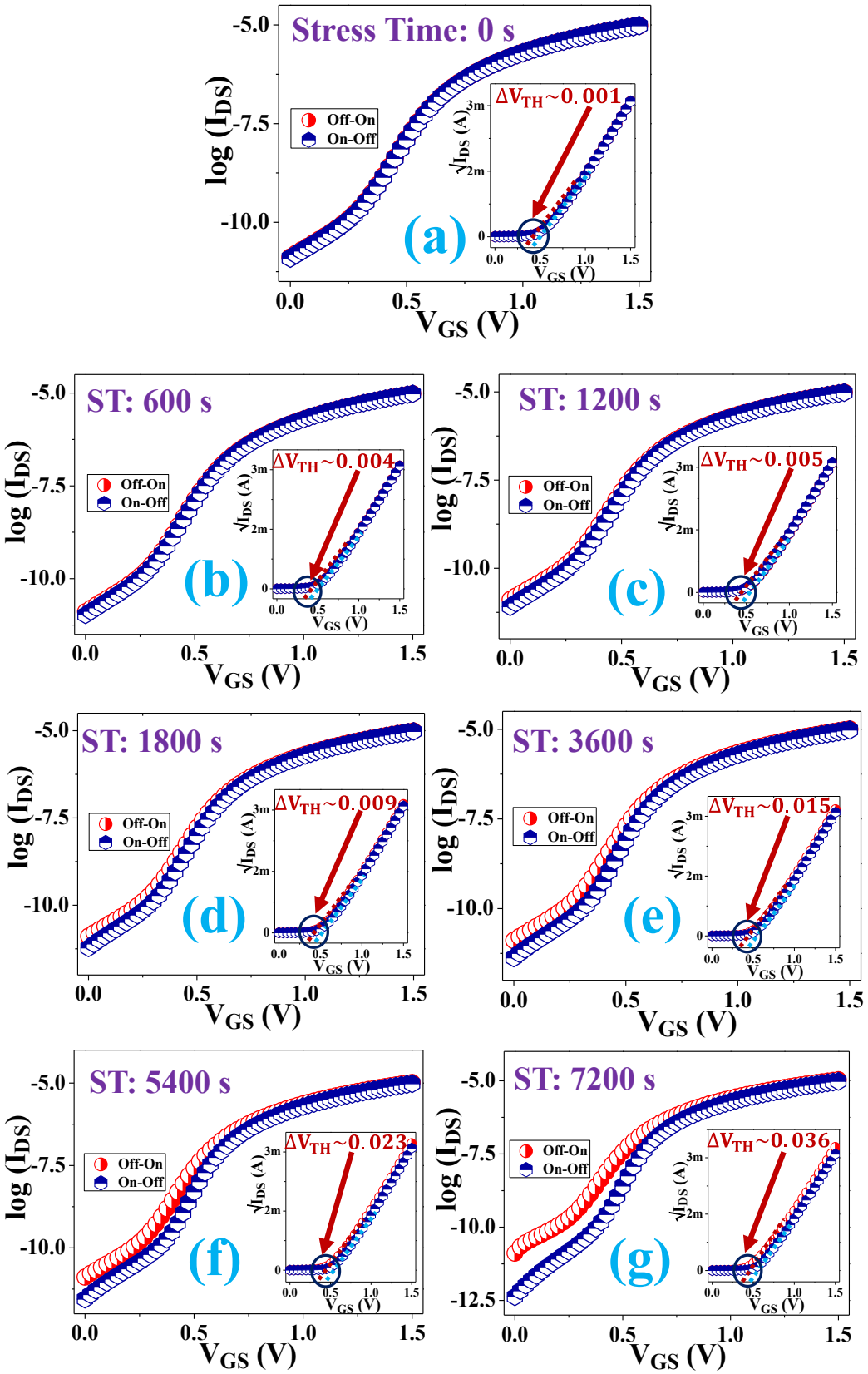


Figure 6.6 (a)-(g) Displays the transfer characteristics for different stress time, when

active layer thickness and dielectric thickness are taken as 30 nm and 60 nm.

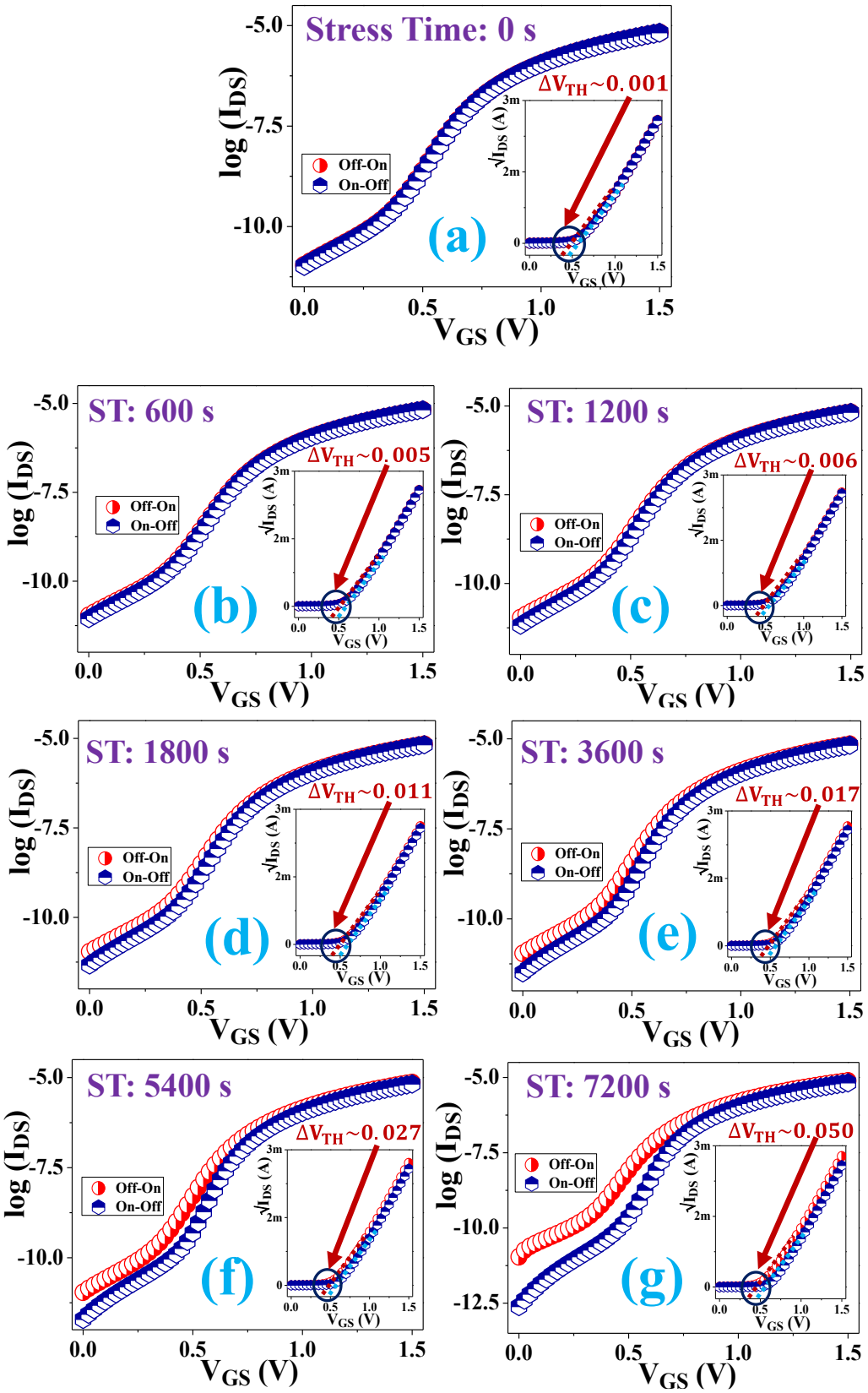


Figure 6.7 (a)-(g) Displays the transfer characteristics for different stress time, when

active layer thickness and dielectric thickness are taken as 30 nm and 70 nm.

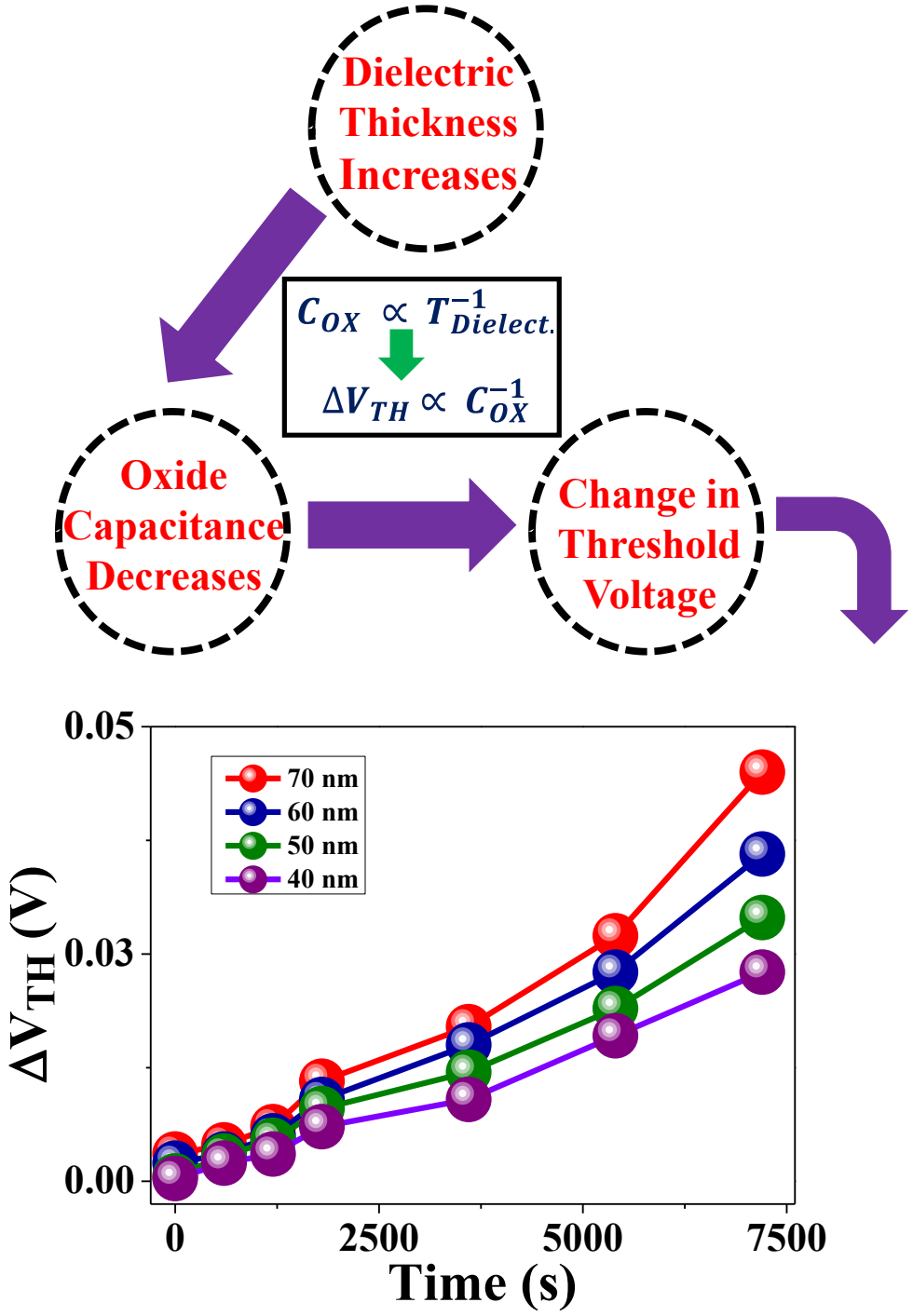


Figure 6.8 Showing the change in ΔV_{TH} with respect to time for dielectric thickness of 40/50/60/ 70 nm.

To operate the device in low operating voltage can be obtained by using high-k dielectric and diminishing dielectric layer thickness ($T_{dielectric}$) [274], [275]. ($T_{dielectric}$) also

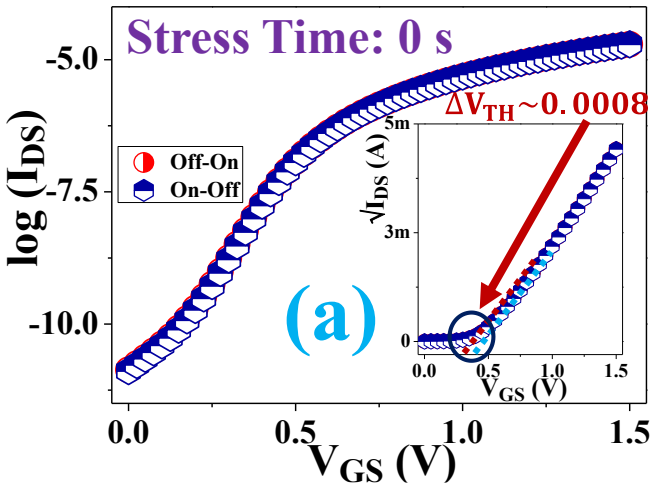
impacts the variation in V_{TH}, as the increase in gate dielectric thickness blocks the injection of charge from the gate side and increases the effect of charge from the channel [270]. Oxide capacitance (C_{OX}) is inversely related to the dielectric thickness and change in threshold voltage (ΔV_{TH}) shown in equations 6.4 and 6.5. **Figure 6.8.** Confirm the variation in the V_{TH} with respect to the increase in dielectric thickness. Among all 4 cases for thickness 40 nm, the minimum for all the stress conditions seems to be the best thickness to be opted for the device.

$$C_{OX} = {}^{\varepsilon}/_{T_{dielectric}} \qquad (6.4)$$

$$\Delta V_{TH} = {}^{qN_T}/_{C_{OX}} \qquad (6.5)$$

B. Variation in the Active layer Thickness

The thickness of active layer ($T_{channel}$) of the oxide TFT played a crucial role that impacted the device's performance and its stability [276]. To examine the behavior of the hysteresis curve in which the change in threshold voltage is calculated for the device, the same procedure is done as performed in the above-mentioned part. In this case, the alteration in the thickness of the active layer (30/20/10 nm) is performed to analyze (ΔV_{TH}) on different thicknesses, which is shown in **Figures. 6.9 and 6.10.**



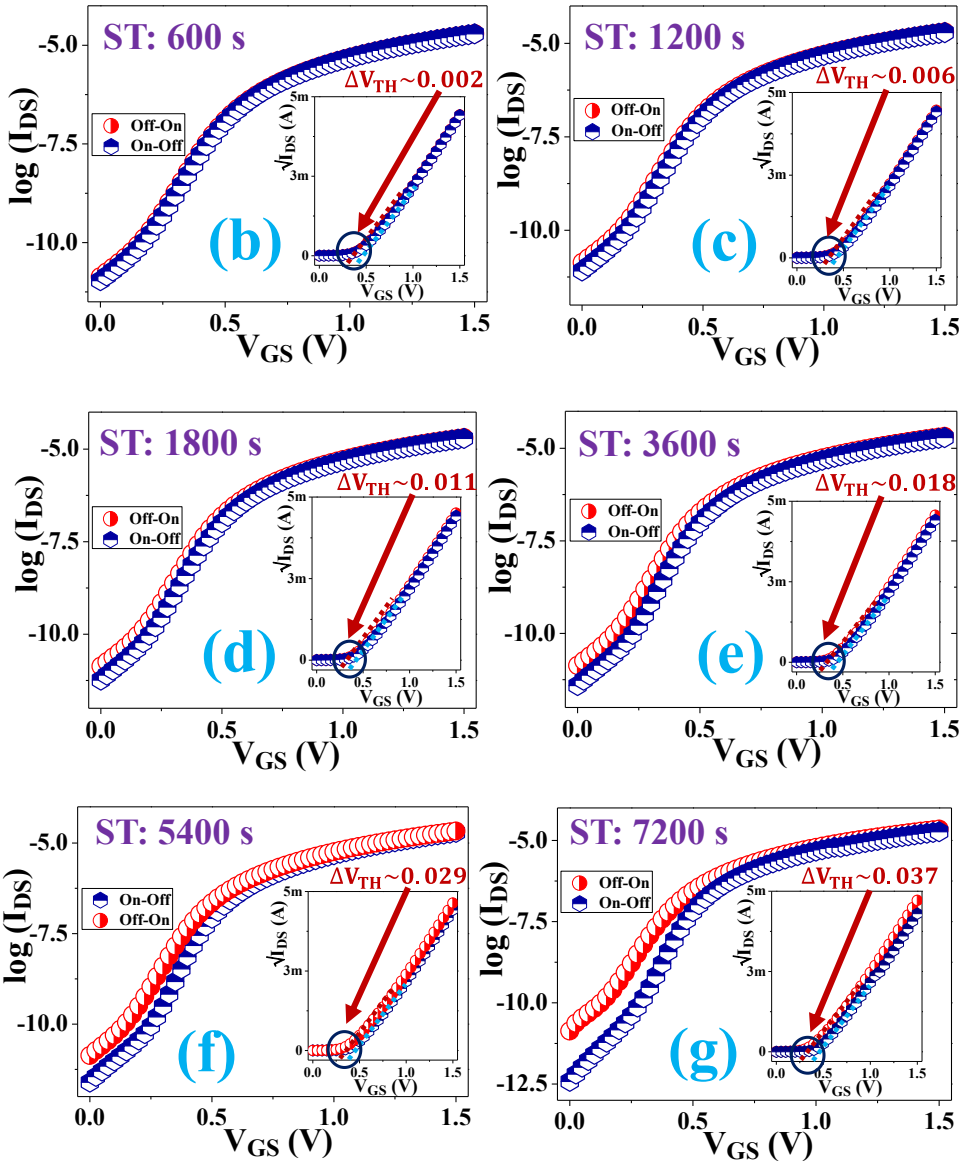
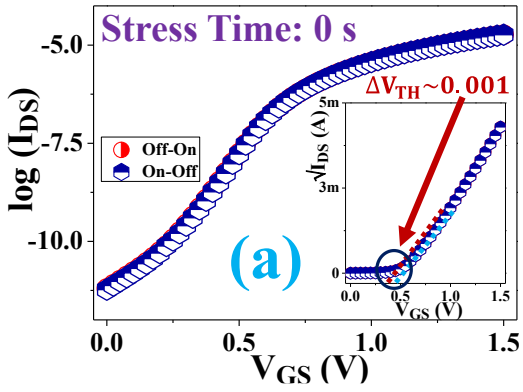


Figure 6.9 (a)-(g) Displays the transfer characteristics for different stress time for the evaluation of ΔV_{TH}, when active layer thickness and dielectric thickness are taken as 20 nm and 40 nm respectively.



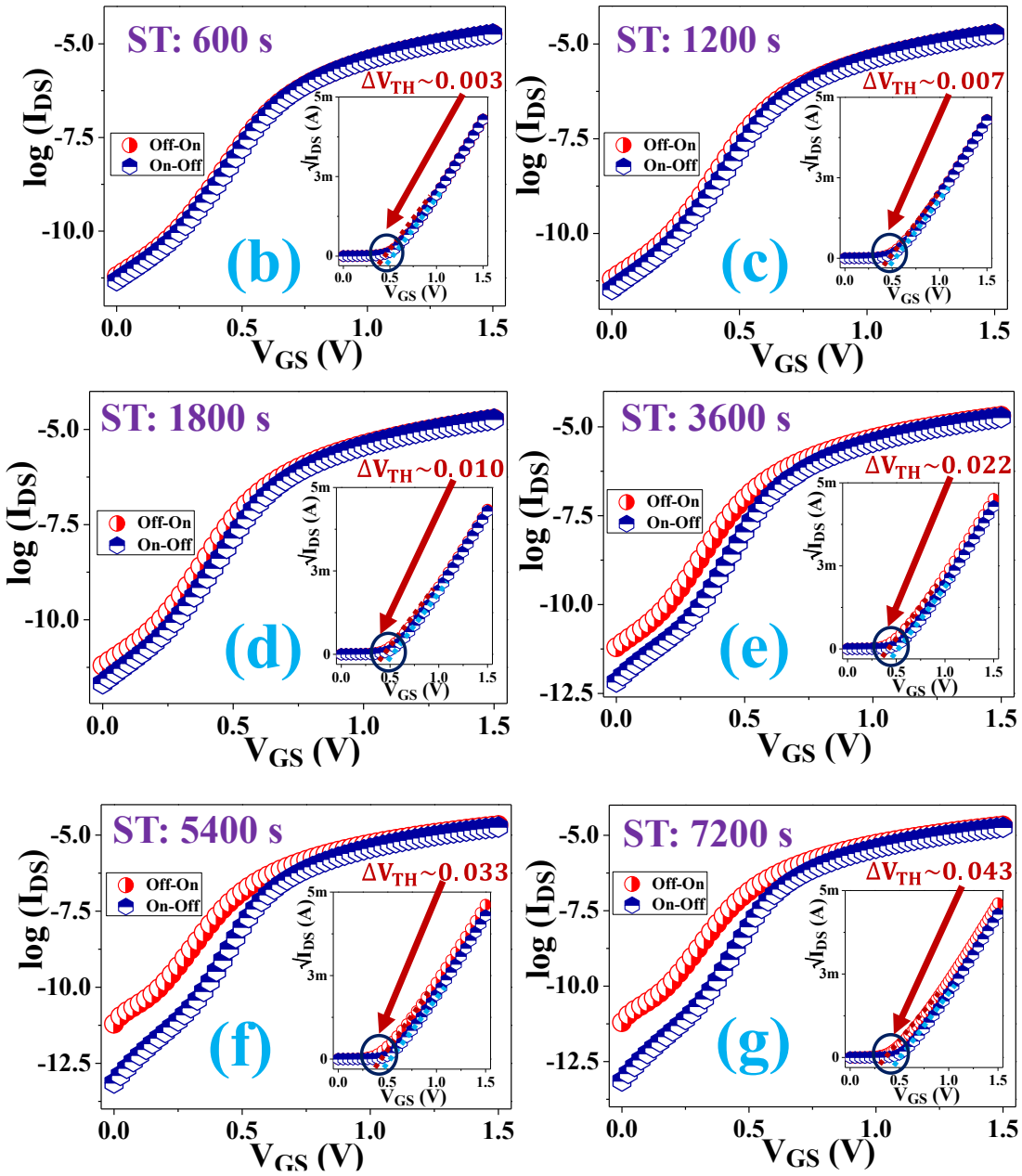


Figure 6.10 (a)-(g) Displays the transfer characteristics for different stress time for the evaluation of ΔV_{TH}, when active layer thickness and dielectric thickness are taken as 10 nm and 40 nm respectively.

The enhanced active layer thickness ($T_{channel}$) improves the PBS stability of TFT as thickness increases, displaces the (V_{TH}) to the left side from the right side [194], [277]. On varying the channel thickness, it directly impacted the bulk states density (N_{Bulk}), which resulted in an enhancement in total trap density (N_T) and alter the threshold voltage

(ΔV_{TH}) [271], [272].

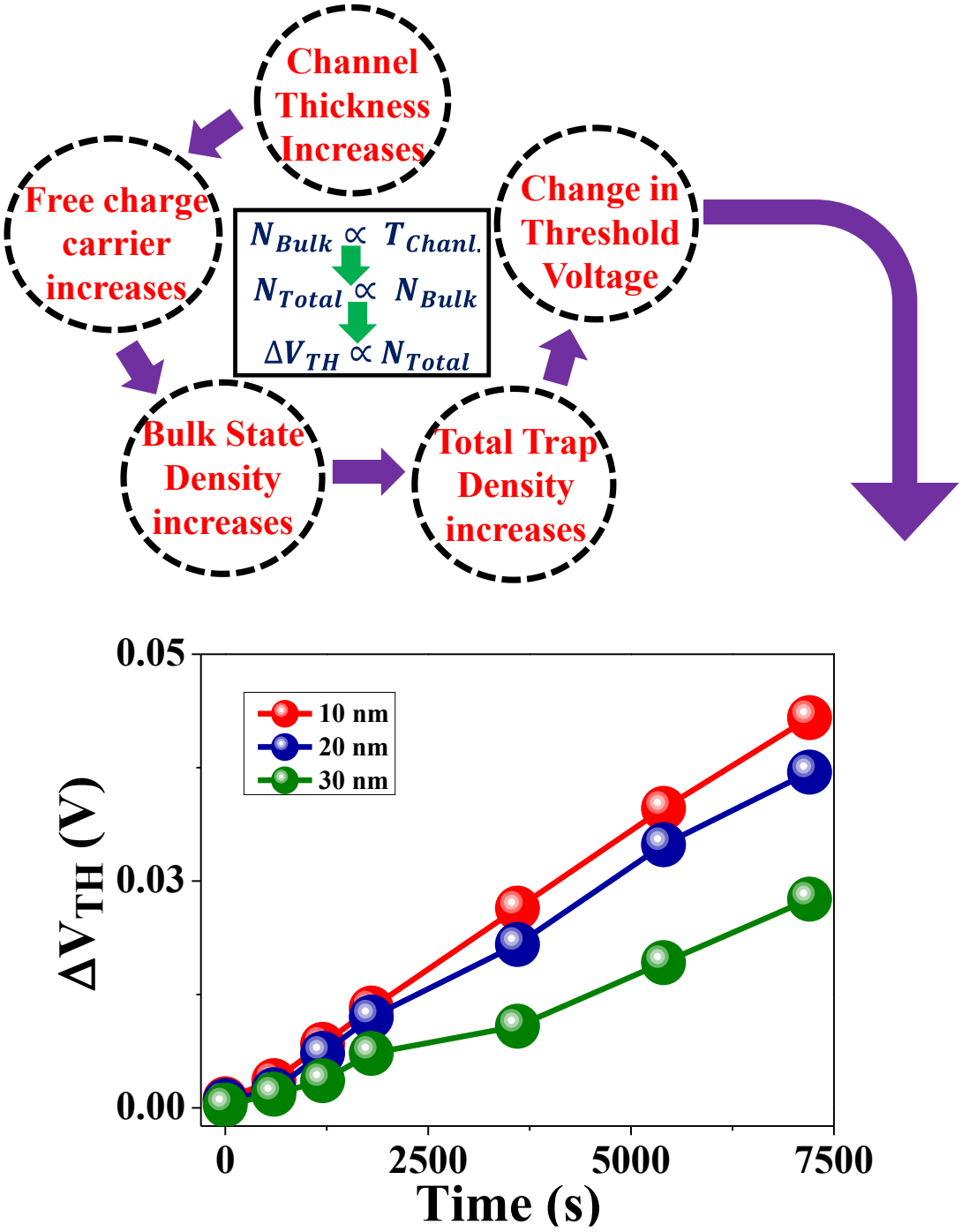


Figure 6.11 Showing the variation of ΔV_{TH} with respect to time for active layer thickness of 30/20/10 nm.

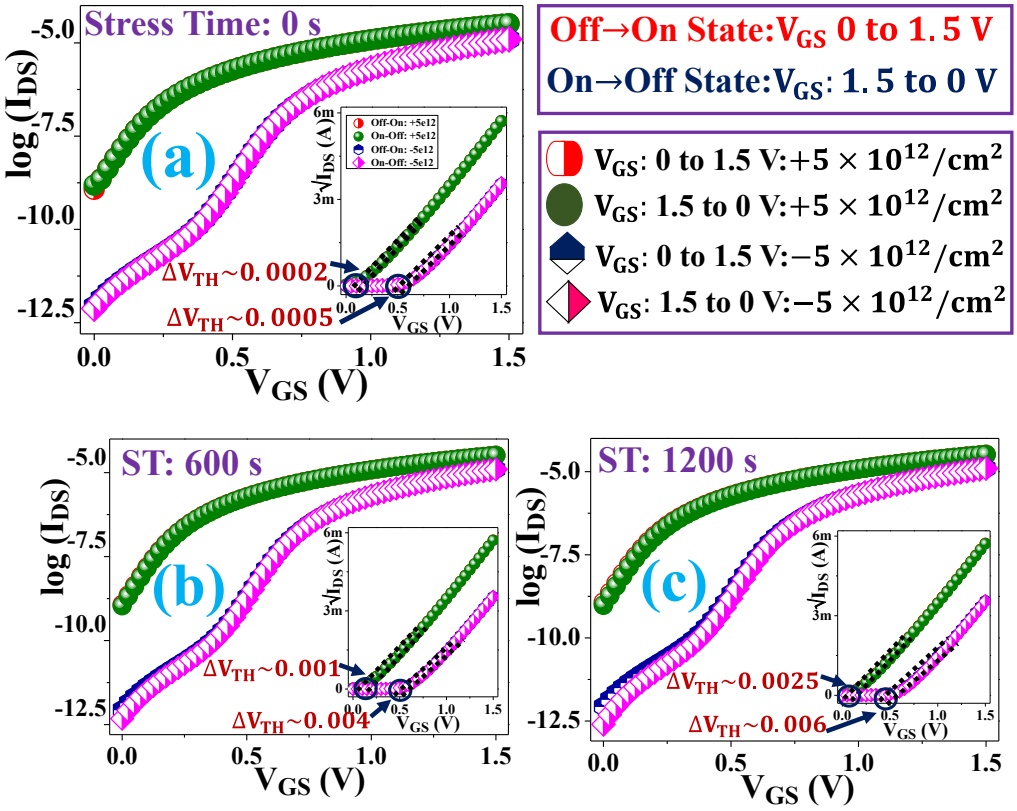
$$N_T = N_{it} + N_{Bulk} \quad (6.6)$$

$$N_{Bulk} \, \alpha \, T_{channel} \quad (6.7)$$

The relationship between and V_{TH} is expressed in equation (6.5). With the help of **Figure 6.11**. V_{TH} is minimum for the active layer thickness of 30nm for all the stress conditions.

C. Variation in the Fixed Charge density In Dielectric

When fixed charge density varies as $\pm 1 \times 10^{12}$ and $\pm 5 \times 10^{12}$ cm^{-2}, the impact on the hysteresis curve is observed in **Figures 6.12 and 6.13**.



When fixed charge density are -5×10^{12} and -1×10^{12} cm^{-2}, V_{TH} magnitude increases (0.34, 0.28 V) from the initial condition (0.21 V) when no fixed charge density is introduced. The reason for this is that negative charge density decreases the electron for the accumulation at the semiconductor-insulator interface. Whereas for positive charge density, it varies $+1 \times 10^{12}$ and $+5 \times 10^{12}$ cm^{-2}, and reduces the V_{TH} magnitude (0.116, 0.176 V) as they lead to further increases in the accumulation of electrons at the interface [278].

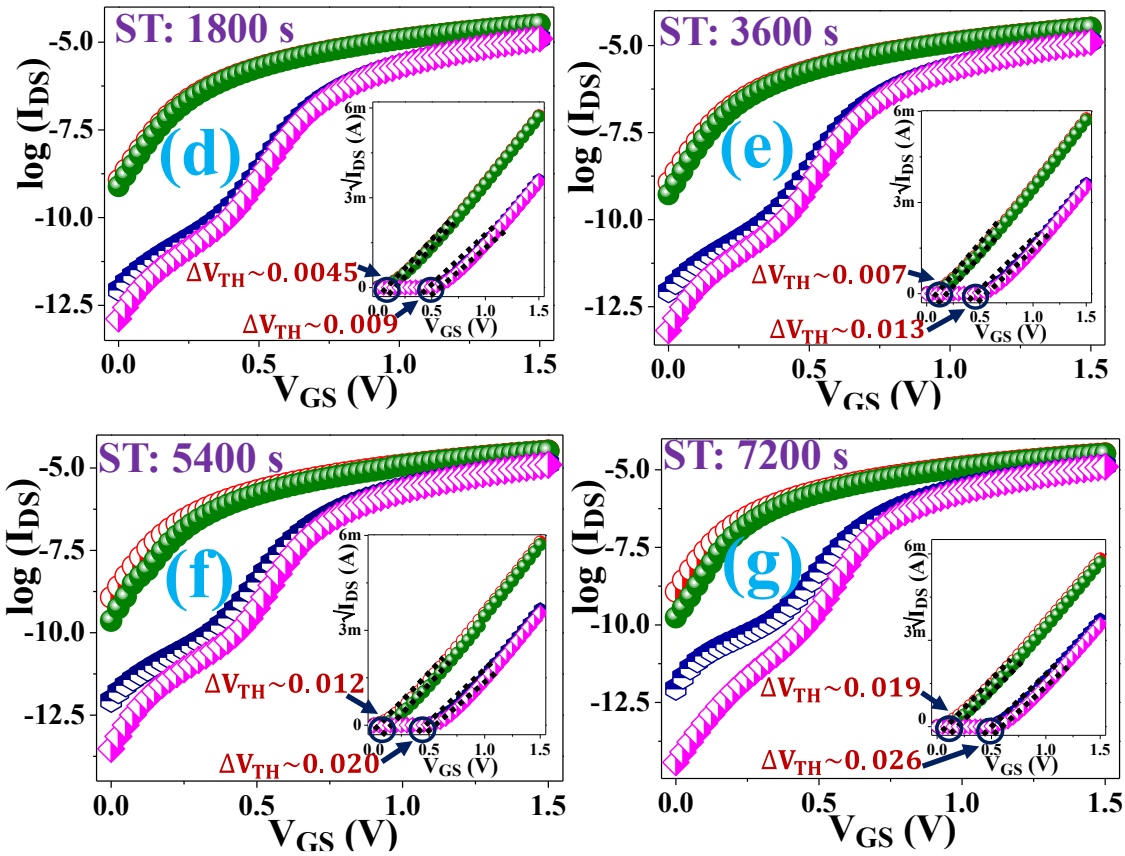
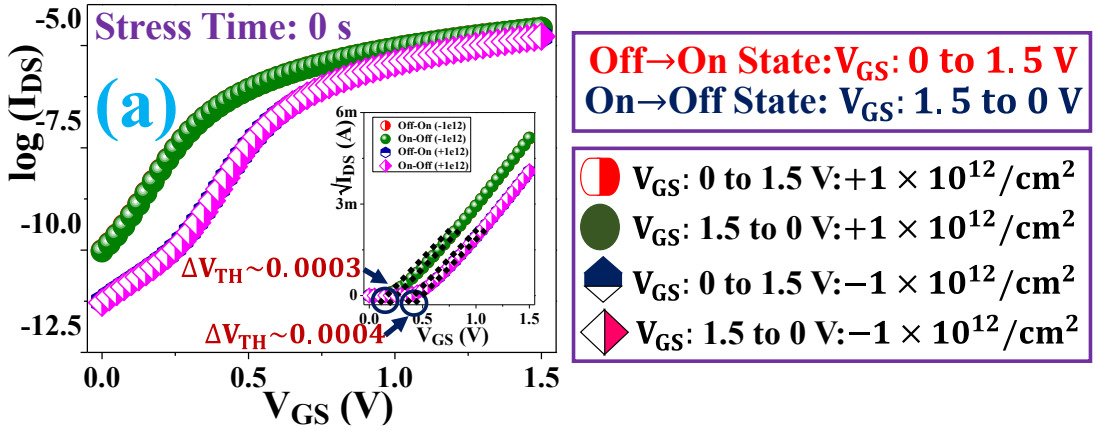


Figure 6.12 (a)-(g) Displays the transfer characteristics for the evaluation of ΔV_{TH}, when fixed charge densities are -5×10^{12} and $+5 \times 10^{12}$ cm^{-2}.



In **Figures 6.12 and 6.13**, both fixed oxide charge densities as $\pm 5 \times 10^{12}$ and $\pm 1 \times 10^{12}$ cm^{-2} are taken together in the same plot to observe that the V_{TH} is tending to move towards the left side for positive fixed charge density and shifted to the right for negative fixed charge density due to alteration of electrons accumulation at surface of the

semiconductor-dielectric interface [278].

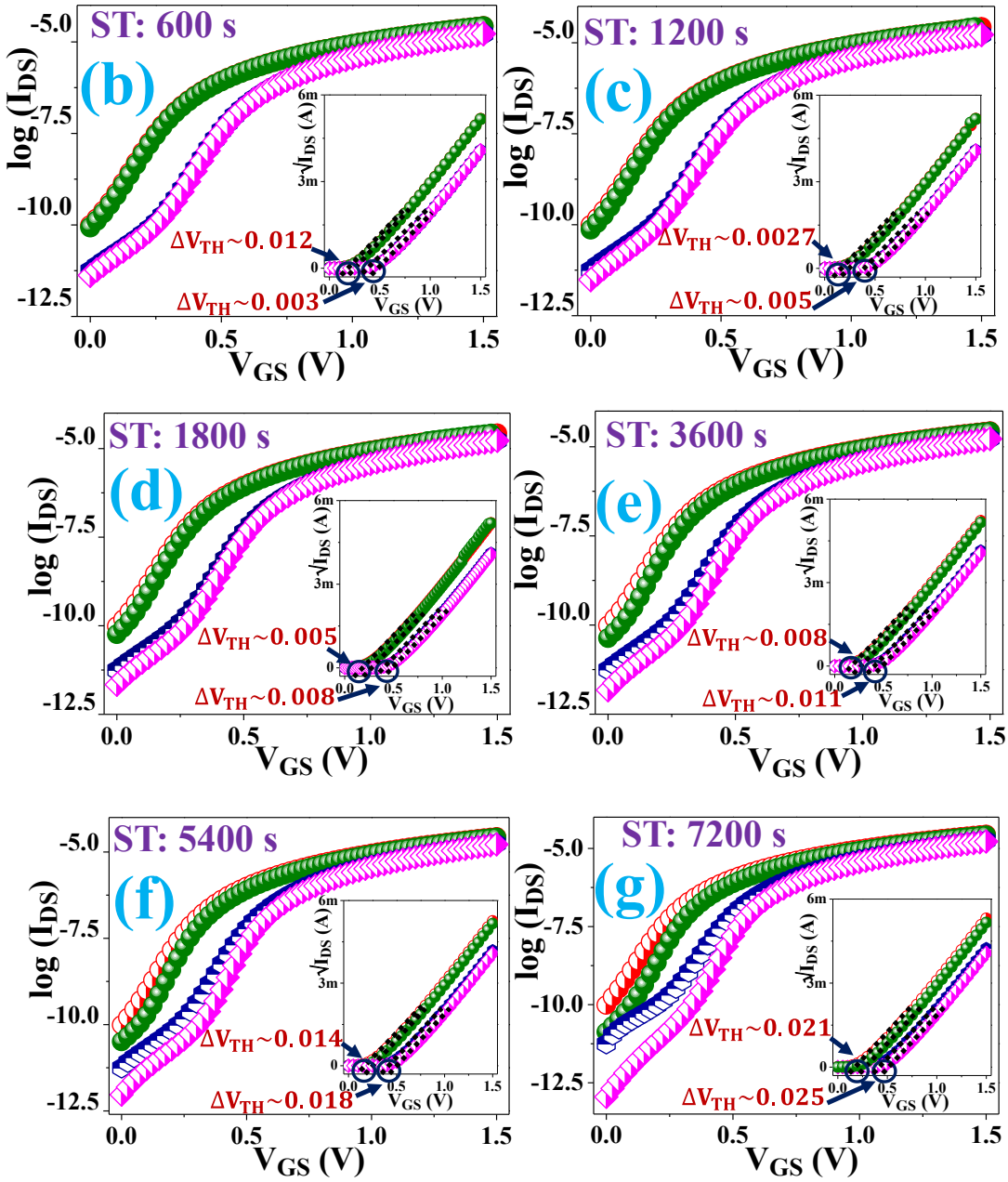


Figure 6.13 (a)-(g) Displays the transfer characteristics for the evaluation of ΔV_{TH}, when fixed charge densities are -1×10^{12} and $+1 \times 10^{12}$ cm^{-2}.

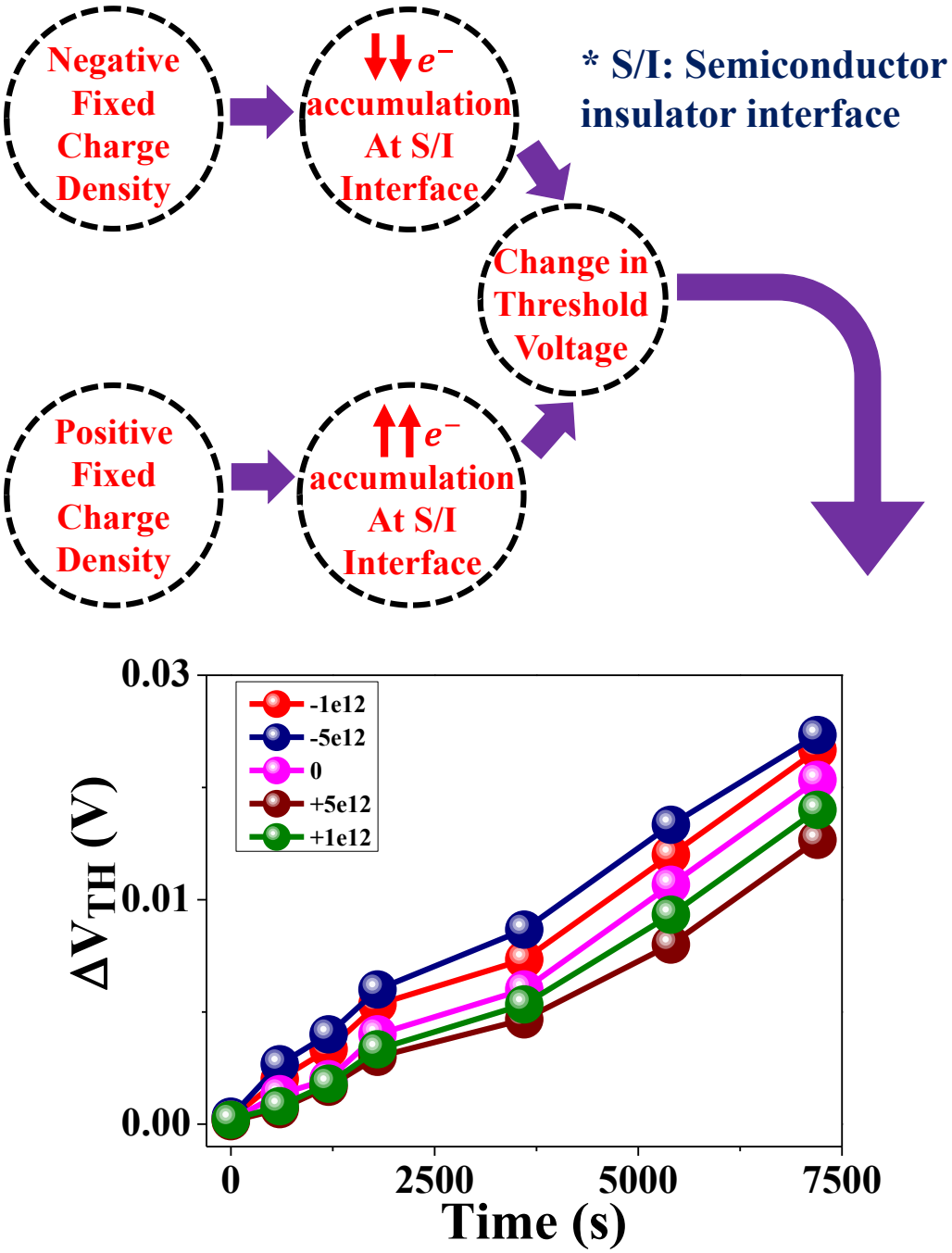


Figure 6.14 Showing the variation of ΔV_{TH} with respect to time for variable fixed charge carrier density.

The variation in V_{TH} has reduced for positive fixed charge density from the initial case and enhanced for negative fixed charge density, these such variation is expressed with the help of **Figure 6.14.** In **Figure 6.15,** Charge trapping is displayed.

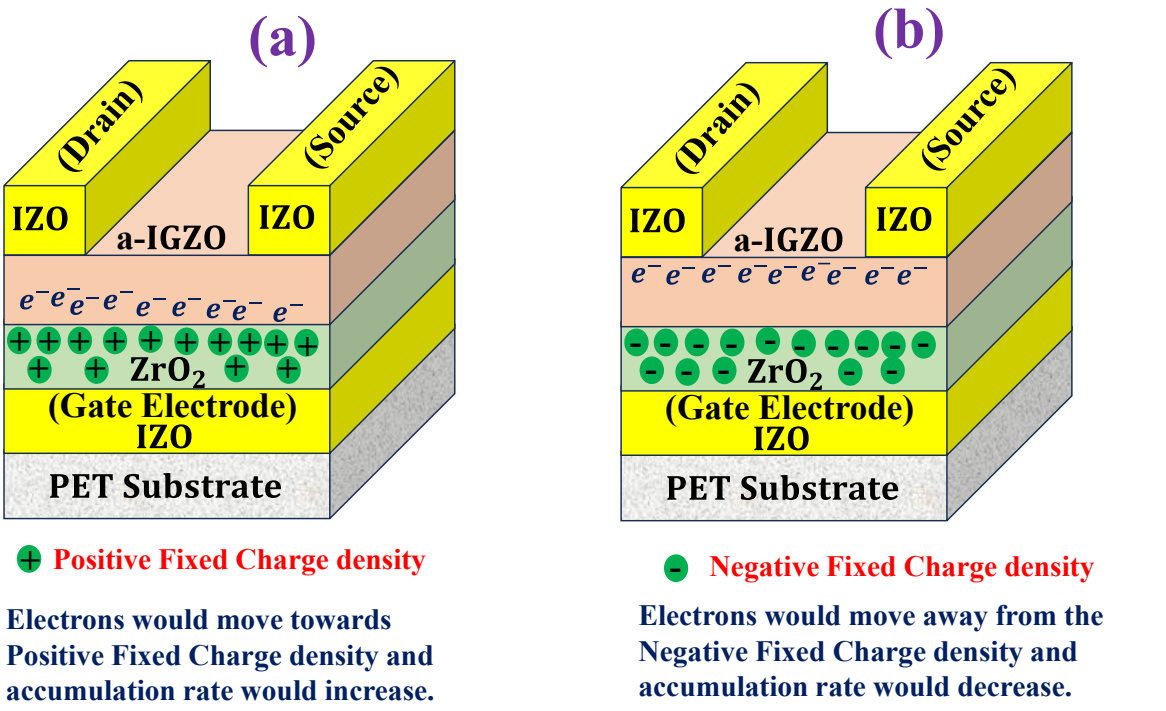
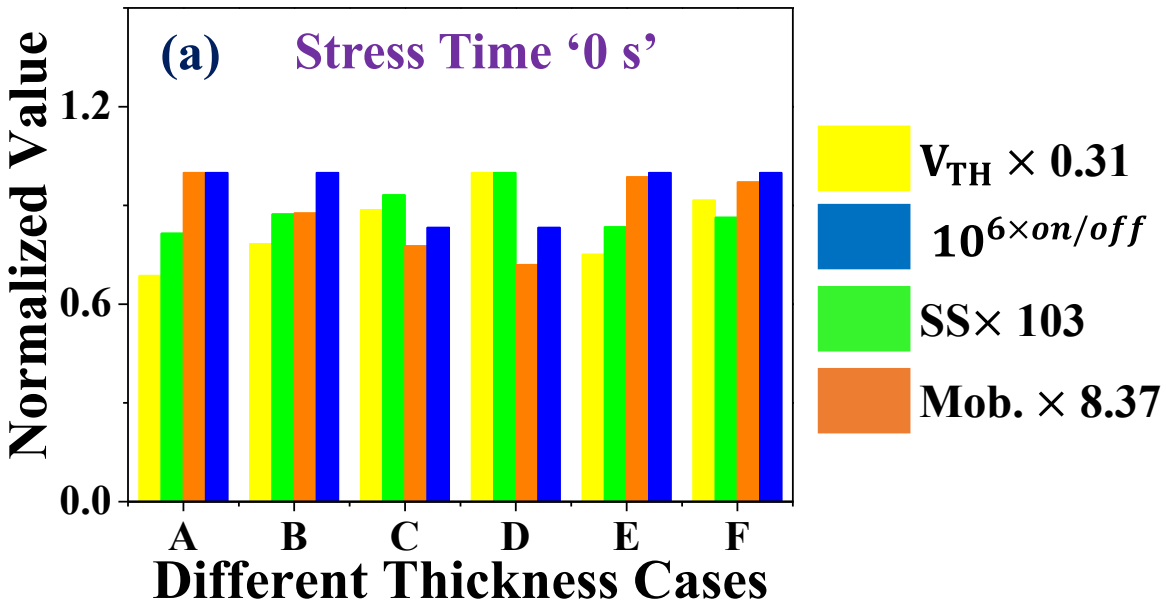
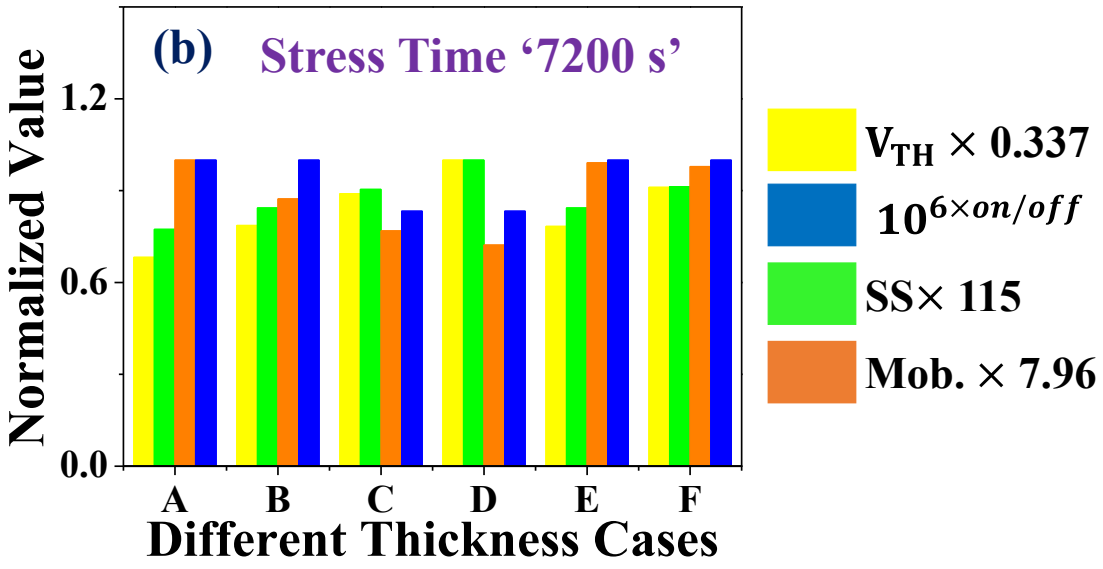


Figure 6.15 (a) and (b) Showing the Charge trapping behaviour for positive and negative fixed charge density.





Cases	A	B	C	D	E	F
T_{AL} (nm)	30	30	30	30	20	10
T_{DL} (nm)	40	50	60	70	40	40

T_{AL}: Active layer thickness T_{DL}: Dielectric layer thickness

Figure 6.16 (a) and (b) Showing the variation of all performance parameters for all different thicknesses of active layer and dielectric layer for stress time '0' and '7200' seconds.

For all cases for different thickness of dielectric and active layer which is expressed in **Figure 6.16 (a) and (b),** case 'A' shows the best among all of them as it has maximum and minimum magnitude of respective parameters according to their desired value.

6.5 Conclusion

In summary, using ZrO_2 dielectric stability analysis has been observed for this a-IGZO-based fully transparent TFT that has been simulated to operate at low-operating voltage. The impact of the thickness of the active layer (10/20/30 nm) and dielectric layer (40/50/60/70 nm) has been observed in estimating the hysteresis curve and in the change

in threshold voltage (ΔV_{TH}) for all different stress times. The results obtained for an active layer thickness and a dielectric thickness of 30 nm and 40 nm show a very small fraction of change in threshold voltage for all the stress times as '0', '600', '1200', '1800', '3600', '5400', and '7200' s. At this thickness, the results of slight variation in threshold voltage (ΔV_{TH}) show improvement in the PBS of this a-IGZO-based TFT. This improved PBS, a highly reliable a-IGZO-based TFT, would be used ahead in realizing complex circuits and flexible electronics.

Chapter 7

Summary and Future Scope

7.1 Summary of all Previous Chapters

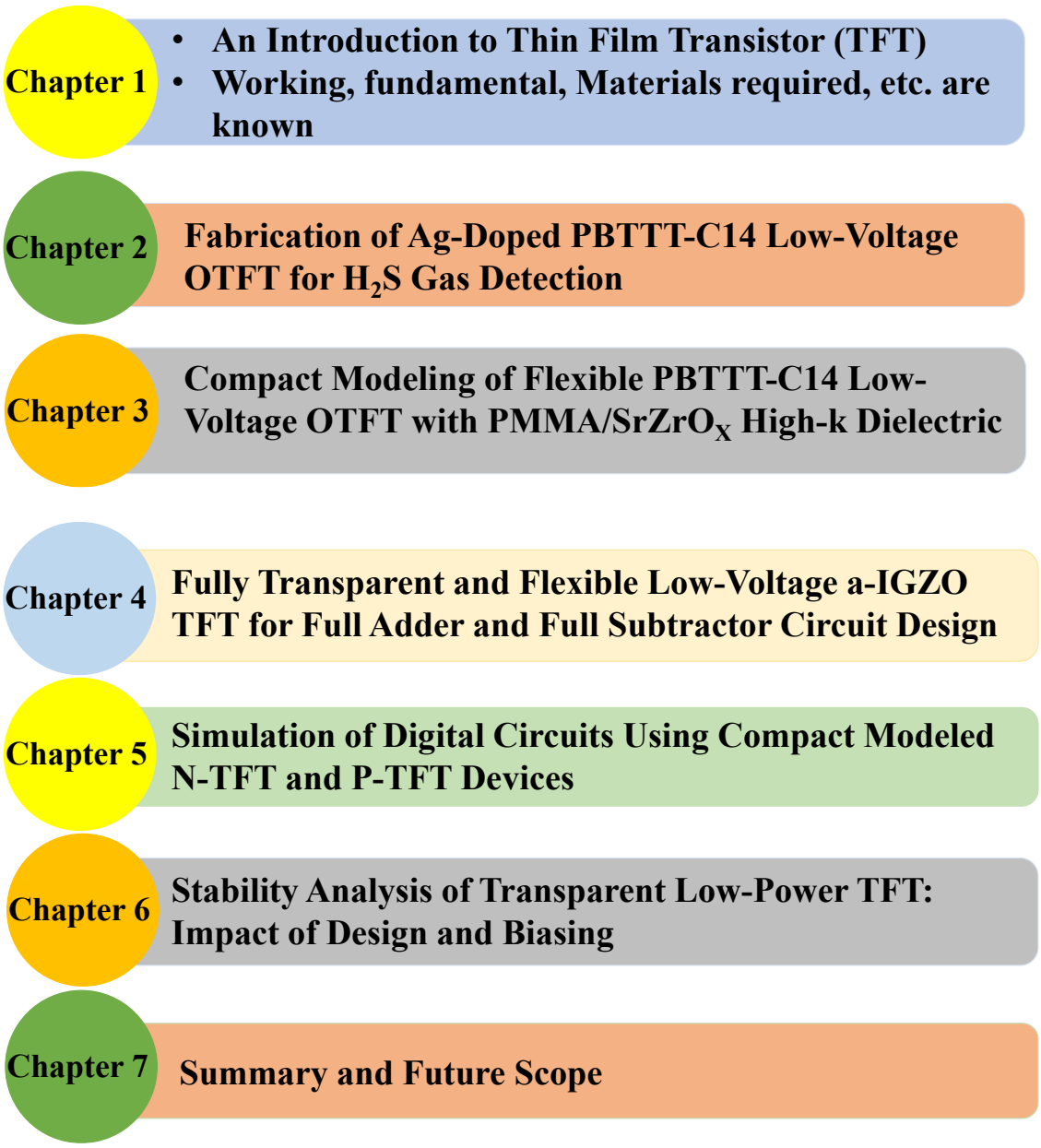


Figure 7.1 Presents the Overview of the Thesis chapters.

The thesis is divided into 7 seven chapters, which are expressed in Figure 7.1. There are many applications of TFT devices. Here the work in the thesis shows TFT for compact

modeling, hydrogen sulfide gas sensing, flexible electronics, and electronic circuit applications.

In **Chapter 1**, an Introduction to thin film transistors (TFTs) is shown, and an investigation of different materials utilized for the establishment of TFTs, the working mechanisms of TFTs, the charge transport phenomenon of organic semiconductors, several techniques used for TFT film deposition, the importance and need for compact modeling of TFT devices, and the role of compact modeling for the implementation of circuits.

Chapter 2 states the fabrication of Ag-doped PBTTT-C14 based OTFT operated at low voltage for the sensing of H_2S gas. The important key points of this chapter are as follows:

1. For the production of cost-effective OTFT devices, methods such as spin coating and floating film transfer (FTM) methods are used for the establishment of a dielectric layer of SrZrOx and an active layer of silver nanoparticles doped PBTTT-C14.
2. This dielectric film exhibits high capacitance of 433 nF/cm², a high bandgap of 4.95 eV, and low-leakage current density of 0.1 nA/cm².
3. This small magnitude of leakage current density assures that this dielectric film has a very small fraction of pinholes, which is favorable for high performance of OTFT.
4. The operation voltage of this Ag-doped PBTTT-C14 OTFT is 1.5 V.
5. This OTFT-based H_2S gas sensor has a sensing response of higher than 80 % and a low limit of detection of ~15.17 ppb.

Chapter 3 states fabrication, characterization, and compact modeling of flexible OTFT devices operated at low voltage for flexible and electronic circuits. The important highlights of this chapter are as follows:

1. The roles of active layer and dielectric layer are played by PBTTT-C14 and the composition of PMMA and $SrZrO_X$.
2. The device has been developed on a PET substrate, which is flexible in nature and helps in developing flexible PBTTT-C14 based OTFT.
3. The atomic force microscopic (AFM) image of the dielectric film shows a uniform smoothness (very low roughness σ_{rms} = 0.407 nm), confirming that the thin film passes with the very low number of surface defects, which is suitable for high-quality transistors.
4. The operating voltage of this flexible OTFT is 1V.
5. The flexible low voltage is compact modeling, which would be used ahead for the implementation of an inverter circuit exhibiting a high gain of 39.77 at V_{DD} ~ -3.6 V.

In **Chapter 4**, a fully transparent, flexible, and low-voltage a-IGZO-based TFT is simulated using the Silvaco Atlas tool. This flexible, transparent TFT compact model is used ahead for further analysis. The essential key points of this chapter are

1. In this fully transparent, flexible TFT, a-IGZO (amorphous indium gallium zinc oxide) and HfO_2 are used as semiconductor and dielectric materials. ITO serves as electrodes for the source, drain, and gate contacts.
2. The device characteristics confirm that operating voltage is 2 V.

3. Using the Silvaco-Techmodeler tool, this simulated device is compact modeled in which the simulated data is verified with the modeled data. Both the curves completely superimpose on each other, ensuring a small error is estimated between the data, which is less than 1%.
4. This compact, modeled, flexible, transparent a-IGZO TFT is used ahead for the realization of full adder and full subtractor circuits using the Silvaco-Gateway tool.
5. Transient analysis is performed, which verifies the truth table for these full adder and subtractor circuits for inputs varying from 000 to 111.

Chapter 5 states the in-depth details associated with the Silvaco-Techmodeler and Silvaco-Gateway tools, and a user guide is developed that states the interlinking of these two tools. Important key points of this chapter are as follows:

1. All the necessary steps related to the Silvaco-Techmodeler tool for the compact modeling of any device are mentioned in a sequential manner.
2. Utilization of this compact modeled device for the implementation of any type of circuitry at the Silvaco-Gateway platform is explained.
3. To check the proper function of the circuit, transient and voltage transfer characteristics are also shown, which are essential to further analysis, such as noise margin analysis, propagation delay estimation, truth table estimation, voltage gain evaluation, etc.
4. Various combination circuits 1-bit magnitude comparator, 1-bit ALU, 2:4 and 3:8 decoders, CMOS inverter circuit, half adder, 4:1 multiplexer, and basic logic gate families are implemented, and respective truth tables and associated parameters are evaluated.

Chapter 6 states the stability analysis of an a-IGZO-based TFT operated at low voltage simulated with the Silvaco-Atlas tool. Positive bias stress (PBS) stability is estimated for different stress times: “0”, “600,” “1200,” “1800,” “3600,” “5400,” and “7200” seconds. Important highlights of this chapter are as follows:

1. The operating voltage of this a-IGZO TFT is 1.5 V.
2. ZrO2 acted as a gate dielectric, and a-IGZO acted as the active layer of this TFT.
3. Impact on variable thickness of active layer (10/20/30 nm) and dielectric layer (70/60/50/40 nm) has been observed on the change in threshold voltage (ΔV_{TH}) for different stress times as 0, “600”, “1200”, “1800”, “3600”, “5400”, and “7200” seconds.
4. Impact of fixed charge density of dielectric on the change in threshold voltage (ΔV_{TH}) for stress times of “0,” “600,” 1200, “1800,” 3600, “5400,” and “7200” seconds.
5. For channel thickness of 30nm and dielectric thickness of 40 nm, very small variation is observed for different stress times.

7.2 Future Scope of the thesis

In the thesis, the research work shown related to device fabrication/simulation for flexible electronics applications, gas sensing applications, and electronics circuits explores various scopes for performing further research analysis related to these fields. Nowadays, there is a hike in the demand for flexible electronics and transparent electronics for several applications; hence, to fulfill these requirements, researchers can work in these domains to develop devices by exploring different materials. Using the compact modeling approach, various memory circuits and transparent op-amp circuits can be realized. In the

field of OTFT, devices can be fabricated for sensing various parameters such as glucose, pH, etc.

References

[1] A. Sharma, C. Madhu, J. S.-I. J. C. Appl, and undefined 2014, "Performance evaluation of thin film transistors: history, technology development and comparison: a review," *Res. Sharma, C Madhu, J SinghInt. J. Comput. Appl, 2014•researchgate.net*, vol. 89, no. 15, pp. 36–40, Mar. 2014, doi: 10.5120/15710-4603.

[2] P. K. Weimer, "The TFT—A New Thin-Film Transistor," *Proc. IRE*, vol. 50, no. 6, pp. 1462–1469, 1962, doi: 10.1109/JRPROC.1962.288190.

[3] S. Oktyabrsky and P. D. Ye, "Fundamentals of III-V semiconductor MOSFETs," *Fundam. III-V Semicond. MOSFETs*, pp. 1–445, 2010, doi: 10.1007/978-1-4419-1547-4/COVER.

[4] S. H., "Synthesis of electrically conducting organic polymers : halogen derivatives of polyacetylene, (CH)x," *Chem. Commun.*, vol. 57, pp. 343-, 1986, Accessed: Jun. 09, 2025. [Online]. Available: https://cir.nii.ac.jp/crid/1572261549846169472

[5] "Organic Electronics: Materials, Manufacturing, and Applications - Google Books." https://books.google.co.in/books?hl=en&lr=&id=Fr016RFJX2MC&oi=fnd&pg=PR5&dq=H.+K.+(Ed.),+Organic+Electronics:+Materials,+Manufacturing+and+Applications,+Wiley-VCH,+Weinheim.+,+2006.+&ots=3MJ07Vq8j2&sig=LsD1ZNzSgiAIRrIat1nc0q6bDZs&redir_esc=y#v=onepage&q&f=false (accessed Jun. 09, 2025).

[6] P. G. Le Comber, W. E. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electron. Lett.*, vol. 15, no. 6, pp. 179–181, Mar. 1979, doi: 10.1049/EL:19790126.

[7] W. E. Spear and P. G. Le Comber, "Substitutional doping of amorphous silicon," *Solid State Commun.*, vol. 17, no. 9, pp. 1193–1196, Nov. 1975, doi: 10.1016/0038-1098(75)90284-7.

[8] W. E. Spear and P. G. Le Comber, "Electronic properties of substitutionally doped amorphous Si and Ge," *Philos. Mag.*, vol. 33, no. 6, pp. 935–949, 1976,

doi: 10.1080/14786437608221926.

[9] C. W. Tang and S. A. Vanslyke, “Organic electroluminescent diodes,” *Appl. Phys. Lett.*, vol. 51, no. 12, pp. 913–915, Sep. 1987, doi: 10.1063/1.98799.

[10] T. Nagayasu *et al.*, “14-in.-diagonal full-color A-Si TFT LCD,” pp. 56–58, 1988, doi: 10.1109/DISPL.1988.11274.

[11] 罪γ *et al.*, “40.1:Active Matrix Low Temperature Poly-Si TFT/OLED Full Color Displays:Development States(2-2.セッション40 OLED DEVICES)(Society for Information Display 00 Report),” p. 66, Jul. 2000, doi: 10.11485/ITETR.24.42.0_66_1.

[12] “Active Matrix Liquid Crystal Displays: Fundamentals and Applications - Willem den Boer - Google Books.” https://books.google.co.in/books?hl=en&lr=&id=EdEzJYJFyU0C&oi=fnd&pg=PP1&dq=W.+D.+Boer,+Active+Matrix+Liquid+Crystal+Displays+Fundamentals+and+Applications,+Newnes,+2005.+&ots=vYUu4-AShu&sig=v32SMbNtZLyzs9c4v3Ydd5Nw2QU&redir_esc=y#v=onepage&q&f=false (accessed Jun. 09, 2025).

[13] “Thin Film Transistors: Materials and Processes | SpringerLink.” https://link.springer.com/book/9781402075049 (accessed Jun. 09, 2025).

[14] S. O. Mbam, S. E. Nwonu, O. A. Orelaja, U. S. Nwigwe, and X. F. Gou, “Thin-film coating; historical evolution, conventional deposition technologies, stress-state micro/nano-level measurement/models and prospects projection: a critical review,” *Mater. Res. Express*, vol. 6, no. 12, p. 122001, Nov. 2019, doi: 10.1088/2053-1591/AB52CD.

[15] S. Y. Yoon, J. Y. Oh, C. O. Kim, and J. Jang, “Low temperature solid phase crystallization of amorphous silicon at 380 °C,” *J. Appl. Phys.*, vol. 84, no. 11, pp. 6463–6465, Dec. 1998, doi: 10.1063/1.368887.

[16] A. T. Voutsas, “A new era of crystallization: advances in polysilicon crystallization and crystal engineering,” *Appl. Surf. Sci.*, vol. 208–209, no. 1, pp. 250–262, Mar. 2003, doi: 10.1016/S0169-4332(02)01343-0.

[17] H. A. Klasens and H. Koelmans, “A tin oxide field-effect transistor,” *Solid State*

Electron., vol. 7, no. 9, pp. 701–702, 1964, doi: 10.1016/0038-1101(64)90057-7.

[18] G. F. Boesen and J. E. Jacobs, "ZnO Field-Effect Transistor," *Proc. IEEE*, vol. 56, no. 11, pp. 2094–2095, 1968, doi: 10.1109/PROC.1968.6813.

[19] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *Science (80-.).*, vol. 300, no. 5623, pp. 1269–1272, May 2003, doi: 10.1126/SCIENCE.1083212/ASSET/BCBAA259-F99C-4433-A0EA-A7E00EC39FE5/ASSETS/GRAPHIC/SE2031534004.JPEG.

[20] J. F. Wager, "Transparent electronics," *Science (80-.).*, vol. 300, no. 5623, pp. 1245–1246, May 2003, doi: 10.1126/SCIENCE.1085276/ASSET/64B30E08-5CAE-4708-A202-253B0FAACA58/ASSETS/GRAPHIC/1245-1.GIF.

[21] E. M. C. Fortunato *et al.*, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature," *Appl. Phys. Lett.*, vol. 85, no. 13, pp. 2541–2543, Sep. 2004, doi: 10.1063/1.1790587.

[22] "Introduction to Thin Film Transistors: Physics and Technology of TFTs - S.D. Brotherton - Google Books." https://books.google.co.in/books?hl=en&lr=&id=E0x0Zghk7okC&oi=fnd&pg=PA3&dq=S.+D.+Brotherton,+Introduction+to+Thin+Film:+Physics+and+Technology+of+TFTs,+Springer,+2013.+&ots=phRHKhwBsZ&sig=ERqcj-Gl7_yVDLCkfPG-Qz6gEEY&redir_esc=y#v=onepage&q=S. D. Brotherton%2C Introduction to Thin Film%3A Physics and Technology of TFTs%2C Springer%2C 2013.&f=false (accessed Jun. 09, 2025).

[23] "Transparent Electronics: From Synthesis to Applications - Google Books." https://books.google.co.in/books?hl=en&lr=&id=8KJEHzSryC4C&oi=fnd&pg=PR7&dq=A.+Facchetti+and+T.+Marks,+Transparent+Electronics:+From+Synthesis+to+Applications,+Wiley,+2010&ots=QUZOFQh60K&sig=UXQaBCI_KwnSSuMeZd72F9u32do&redir_esc=y#v=onepage&q=A. Facchetti and T. Marks%2C Transparent Electronics%3A From Synthesis to Applications%2C Wiley%2C 2010&f=false (accessed Jun. 09, 2025).

[24] Y. Hara *et al.*, "IGZO-TFT technology for large-screen 8K display," *J. Soc. Inf. Disp.*, vol. 26, no. 3, pp. 169–177, Mar. 2018, doi: 10.1002/JSID.648.

[25] G. P. Crawford, “Flexible Flat Panel Displays,” *Flex. Flat Panel Displays*, pp. 1–528, Jun. 2005, doi: 10.1002/0470870508.

[26] M. Pope and C. E. Swenberg, “Electronic Processes in Organic Crystals and Polymers,” *Electron. Process. Org. Cryst. Polym.*, Dec. 1999, doi: 10.1093/OSO/9780195129632.001.0001.

[27] G. Malliaras and R. Friend, “An Organic Electronics Primer,” *Phys. Today*, vol. 58, no. 5, pp. 53–58, May 2005, doi: 10.1063/1.1995748.

[28] S. E. Shaheen, C. J. Brabec, N. S. Sariciftci, F. Padinger, T. Fromherz, and J. C. Hummelen, “2.5% efficient organic plastic solar cells,” *Appl. Phys. Lett.*, vol. 78, no. 6, pp. 841–843, Feb. 2001, doi: 10.1063/1.1345834.

[29] P. Peumans, S. Uchida, and S. R. Forrest, “Efficient bulk heterojunction photovoltaic cells using small-molecular-weight organic thin films,” *Nature*, vol. 425, no. 6954, pp. 158–162, Sep. 2003, doi: 10.1038/NATURE01949;KWRD=SCIENCE.

[30] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, “Pentacene organic thin-film transistors - Molecular ordering and mobility,” *IEEE Electron Device Lett.*, vol. 18, no. 3, pp. 87–89, Mar. 1997, doi: 10.1109/55.556089.

[31] C. Santato *et al.*, “Tetracene light-emitting transistors on flexible plastic substrates,” *Appl. Phys. Lett.*, vol. 86, no. 14, pp. 1–3, Apr. 2005, doi: 10.1063/1.1898429/329855.

[32] C. Rost, S. Karg, W. Riess, M. A. Loi, M. Murgia, and M. Muccini, “Ambipolar light-emitting organic field-effect transistor,” *Appl. Phys. Lett.*, vol. 85, no. 9, pp. 1613–1615, Aug. 2004, doi: 10.1063/1.1785290.

[33] H. Meng, Z. Bao, A. J. Lovinger, B. C. Wang, and A. M. Mujsce, “High field-effect mobility oligofluorene derivatives with high environmental stability [1],” *J. Am. Chem. Soc.*, vol. 123, no. 37, pp. 9214–9215, Sep. 2001, doi: 10.1021/JA016525O/SUPPL_FILE/JA016525O_S1.PDF.

[34] R. Zeis *et al.*, “Single-crystal field-effect transistors based on organic selenium-containing semiconductor,” *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short*

Notes Rev. Pap., vol. 44, no. 6 A, pp. 3712–3714, Jun. 2005, doi: 10.1143/JJAP.44.3712/XML.

[35] J. Liu *et al.*, "High mobility emissive organic semiconductor," *Nat. Commun. 2015 61*, vol. 6, no. 1, pp. 1–8, Dec. 2015, doi: 10.1038/ncomms10032.

[36] K. Nomura, T. Kamiya, H. Ohta, K. Ueda, M. Hirano, and H. Hosono, "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline InGaO3(ZnO)5 films," *Appl. Phys. Lett.*, vol. 85, no. 11, pp. 1993–1995, Sep. 2004, doi: 10.1063/1.1788897.

[37] M. W. J. Prins *et al.*, "A ferroelectric transparent thin-film transistor," *Appl. Phys. Lett.*, vol. 68, no. 25, pp. 3650–3652, Jun. 1996, doi: 10.1063/1.115759.

[38] A. Takagi *et al.*, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films*, vol. 486, no. 1–2, pp. 38–41, Aug. 2005, doi: 10.1016/J.TSF.2004.11.223.

[39] C. Bright, "Alternative Transparent Conductive Oxides (TCO) to ITO," 2008.

[40] R. C. G. Naber *et al.*, "High-performance solution-processed polymer ferroelectric field-effect transistors," *Nat. Mater.*, vol. 4, no. 3, pp. 243–248, Feb. 2005, doi: 10.1038/NMAT1329;KWRD=MATERIALS+SCIENCE.

[41] J. S. Lee *et al.*, "Layer-by-layer assembled charge-trap memory devices with adjustable electronic properties," *Nat. Nanotechnol.*, vol. 2, no. 12, pp. 790–795, Dec. 2007, doi: 10.1038/NNANO.2007.380;KWRD=MATERIALS+SCIENCE.

[42] Z. Liu, F. Xue, Y. Su, Y. M. Lvov, and K. Varahramyan, "Memory effect of a polymer thin-film transistor with self-assembled gold nanoparticles in the gate dielectric," *IEEE Trans. Nanotechnol.*, vol. 5, no. 4, pp. 379–384, Jul. 2006, doi: 10.1109/TNANO.2006.876928.

[43] X. Gao, X. J. She, C. H. Liu, Q. J. Sun, J. Liu, and S. D. Wang, "Organic field-effect transistor nonvolatile memories based on hybrid nano-floating-gate," *Appl. Phys. Lett.*, vol. 102, no. 2, Jan. 2013, doi: 10.1063/1.4776677/974875.

[44] R. Capelli, S. Toffanin, G. Generali, H. Usta, A. Facchetti, and M. Muccini, "Organic light-emitting transistors with an efficiency that outperforms the equivalent light-emitting diodes," *Nat. Mater.*, vol. 9, no. 6, pp. 496–503, May

2010, doi: 10.1038/NMAT2751;SUBJMETA=1000,1019,1020,1091,119,301,639,998;KWRD=MOLECULAR+ELECTRONICS,ORGANIC+LEDS,SEMICONDUCTORS.

[45] A. Facchetti, "π-Conjugated polymers for organic electronics and photovoltaic cell applications," *Chem. Mater.*, vol. 23, no. 3, pp. 733–758, Feb. 2011, doi: 10.1021/CM102419Z/ASSET/IMAGES/LARGE/CM-2010-02419Z_0017.JPEG.

[46] † and Yasuhiko Shirota* and H. Kageyama‡, "Charge Carrier Transporting Molecular Materials and Their Applications in Devices," 2007, doi: 10.1021/CR050143+.

[47] H. E. Katz and J. Huang, "Thin-film organic electronic devices," *Annu. Rev. Mater. Res.*, vol. 39, no. Volume 39, 2009, pp. 71–92, Aug. 2009, doi: 10.1146/ANNUREV-MATSCI-082908-145433/CITE/REFWORKS.

[48] J. Kang, N. Shin, Y. J. Do, V. M. Prabhu, and D. Y. Yoon, "Structure and properties of small molecule-polymer blend semiconductors for organic thin film transistors," *J. Am. Chem. Soc.*, vol. 130, no. 37, pp. 12273–12275, Sep. 2008, doi: 10.1021/JA804013N/SUPPL_FILE/JA804013N_SI_001.PDF.

[49] O. Krutko and A. Dodabalapur, "Charge transport and dynamic response of organic and polymer transistors," *J. Appl. Phys.*, vol. 127, no. 10, Mar. 2020, doi: 10.1063/1.5122767/13457716/105501_1_ACCEPTED_MANUSCRIPT.PDF.

[50] F. Jensen, "Introduction to computational chemistry," p. 638, 2017.

[51] "Organic Chemistry, 9th Ed - T. W. Graham Solomons, Craig B. Fryhle - Google Books." https://books.google.co.in/books?hl=en&lr=&id=uUkpzYxMIPAC&oi=fnd&pg=PA1&dq=T.+W.+Graham+Solomons,+Craig+B.+Fryhle,+Scott+A.+Snyder,+Organic+Chemistry,+12th+Edition,+Wiley,+2015.+&ots=EdEwk3qW2a&sig=ft5bAa0ErYoq3ZWhJCRqNKQ_wFQ&redir_esc=y#v=onepage&q&f=false (accessed Jun. 09, 2025).

[52] "Plastic electronics | Coursera." https://www.coursera.org/learn/plastic-electronics (accessed Jun. 09, 2025).

[53] S. H. Mir, L. A. Nagahara, T. Thundat, P. Mokarian-Tabari, H. Furukawa, and A. Khosla, “Review—Organic-Inorganic Hybrid Functional Materials: An Integrated Platform for Applied Technologies,” *J. Electrochem. Soc.*, vol. 165, no. 8, pp. B3137–B3156, May 2018, doi: 10.1149/2.0191808JES/XML.

[54] “L. Petti et al., “Metal oxide semiconductor thin-film... - Google Scholar.” https://scholar.google.com/scholar?hl=en&as_sdt=0%2C5&q=L.+Petti+et+al.%2C+“Metal+oxide+semiconductor+thin-film+transistors+for+flexible+electronics%2C”+Applied+Physics+Reviews%2C+vol.+3%2C+no.+2%2C+2016.+&btnG= (accessed Jun. 09, 2025).

[55] S. M. . Sze, “Semiconductor devices : Physics and technology,” p. 564, 2009.

[56] K. A. Jenkins, J. Y. C. Sun, and J. Gautier, “History dependence of output characteristics of silicon-on-insulator (SOI) MOSFET’s,” *IEEE Electron Device Lett.*, vol. 17, no. 1, pp. 7–9, Jan. 1996, doi: 10.1109/55.475560.

[57] “Thin-Film Transistors,” *Thin-Film Transistors*, Feb. 2003, doi: 10.1201/9780203911778.

[58] M. S. Mehrolia, D. Kumar, A. Verma, and A. K. Singh, “Fabrication and Compact Modeling of Low-Voltage Flexible Organic TFT Using Self-Assembly of Conductive Polymer Channel Over High- *k* PMMA/SrZrO$_{\textit{x}}$ Dielectric,” *IEEE Trans. Electron Devices*, pp. 1–6, 2024, doi: 10.1109/TED.2024.3442165.

[59] M. S. Mehrolia, D. Kumar, A. Verma, and A. K. Singh, “Fabrication and Characterization of Self-Assembled Low Voltage Operated OTFT for H2S Gas Sensor for Oil and Gas Industry,” *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 769–776, Jan. 2024, doi: 10.1109/TED.2023.3336301.

[60] “Handbook of Deposition Technologies for Films and Coatings: Science ... - Peter M. Martin - Google Books.” https://books.google.co.in/books?hl=en&lr=&id=k9mXGyFPFGoC&oi=fnd&pg=PP2&dq=P.+M.+Martin,+Handbook+of+Deposition+Technologies+for+Films+and+Coatings,+Elsevier,+2010.+&ots=-AdJNDquwm&sig=onTvVi9hVCXyculQ4T7DesAz2Dk&redir_esc=y#v=onepage&q&f=false (accessed Jun. 09, 2025).

[61] “Chemical Vapour Deposition (CVD): Advances, Technology and Applications - Google Books.” https://books.google.co.in/books?hl=en&lr=&id=NiGeDwAAQBAJ&oi=fnd&pg=PP1&dq=K.+L.+Choy,+Chemical+Vapour+Deposition+(CVD)+Advances,+Technology+and+Applications,+CRC+Press,+2019.+&ots=bJQ7k9KW1J&sig=Gpyr7vPNY4so-wouGV9WFwo2tY0&redir_esc=y#v=onepage&q=K. L. Choy%2C Chemical Vapour Deposition (CVD) Advances%2C Technology and Applications%2C CRC Press%2C 2019.&f=false (accessed Jun. 09, 2025).

[62] S. M. Rossnagel, “Thin film deposition with physical vapor deposition and related technologies,” *J. Vac. Sci. Technol. A*, vol. 21, no. 5, pp. S74–S87, Sep. 2003, doi: 10.1116/1.1600450.

[63] T. Schneller, R. Waser, M. Kosec, and D. Payne, “Chemical solution deposition of functional oxide thin films,” *Chem. Solut. Depos. Funct. Oxide Thin Film.*, vol. 9783211993118, pp. 1–796, Dec. 2013, doi: 10.1007/978-3-211-99311-8/COVER.

[64] C. Kumar and S. Jit, “Blended PQT-12 and PC61BM Thin Films Based Self-Powered and Fast Response Photodetector,” *IEEE Electron Device Lett.*, vol. 41, no. 10, pp. 1556–1559, Oct. 2020, doi: 10.1109/LED.2020.3018035.

[65] D. D. Deshmukh and V. D. Kalyankar, “Deposition Characteristics of Multitrack Overlayby Plasma Transferred Arc Welding on SS316Lwith Co-Cr Based Alloy-Influence ofProcess Parameters,” *High Temp. Mater. Process.*, vol. 38, no. 2019, pp. 248–263, Jan. 2019, doi: 10.1515/HTMP-2018-0046/ASSET/GRAPHIC/J_HTMP-2018-0046_FIG_007.JPG.

[66] V. K. Champagne, “The cold spray materials deposition process,” *(No Title)*, pp. 1–362, 2007, doi: 10.1533/9781845693787.

[67] “NRL Review - Google Books.” https://books.google.co.in/books?hl=en&lr=&id=0TMk-N0OhCIC&oi=fnd&pg=PA73&dq=D.+Chrisey+and+G.+Hubler+,+Pulsed+Laser+Deposition+of+Thin+Films,+Wiley–Blackwell,+1994.+&ots=QWorNM2XEL&sig=8KXvVMxjUG7wUUVWX6lUa2UjzwE&redir_esc=y#v=onepage&q&f=false (accessed Jun. 09, 2025).

[68] S. Jana, R. K. Pandey, and R. Prakash, “Evolution of Edge-On Oriented Polymer Films Self-Assembled at the Air-Liquid Interface for High-Performance Electronic Device Applications,” *ACS Appl. Polym. Mater.*, vol. 4, no. 7, pp. 4818–4828, Jul. 2022, doi: 10.1021/ACSAPM.2C00414/ASSET/IMAGES/LARGE/AP2C00414_0006.JPEG.

[69] J. Li *et al.*, “An Improved Large Signal Model for 0.1 μm AlGaN/GaN High Electron Mobility Transistors (HEMTs) Process and Its Applications in Practical Monolithic Microwave Integrated Circuit (MMIC) Design in W band,” *Micromachines 2018, Vol. 9, Page 396*, vol. 9, no. 8, p. 396, Aug. 2018, doi: 10.3390/MI9080396.

[70] K. Han, G. Qiao, Z. Deng, and Y. Zhang, “Asymmetric Drain Extension Dual-kk Trigate Underlap FinFET Based on RF/Analog Circuit,” *Micromachines 2017, Vol. 8, Page 330*, vol. 8, no. 11, p. 330, Nov. 2017, doi: 10.3390/MI8110330.

[71] P. Buccella *et al.*, “Methodology for 3-D Substrate Network Extraction for SPICE Simulation of Parasitic Currents in Smart Power ICs,” *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 35, no. 9, pp. 1489–1502, Sep. 2016, doi: 10.1109/TCAD.2015.2513008.

[72] H. Cheng *et al.*, “A review for compact model of graphene field-effect transistors*,” *Chinese Phys. B*, vol. 26, no. 3, p. 036804, Mar. 2017, doi: 10.1088/1674-1056/26/3/036804.

[73] N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li, and M. Liu, “A Review for Compact Model of Thin-Film Transistors (TFTs),” *Micromachines 2018, Vol. 9, Page 599*, vol. 9, no. 11, p. 599, Nov. 2018, doi: 10.3390/MI9110599.

[74] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, “Organic thin-film transistors: Part I-compact DC modeling,” *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2952–2961, Dec. 2009, doi: 10.1109/TED.2009.2033308.

[75] T. Kacprzak and A. Materka, “Compact dc Model of GaAs FET’s for Large-Signal Computer Calculation,” *IEEE J. Solid-State Circuits*, vol. 18, no. 2, pp. 211–213, 1983, doi: 10.1109/JSSC.1983.1051924.

[76] S. S. Ahmed, D. M. Kim, and H. Shichijo, “A Comprehensive Analytic Model of

Accumulation-Mode MOSFET's in Polysilicon Thin Films," *IEEE Trans. Electron Devices*, vol. 33, no. 7, pp. 973–985, 1986, doi: 10.1109/T-ED.1986.22603.

[77] B. Iñiguez, Z. Xu, T. A. Fjeldly, and M. S. Shur, "Unified model for short-channel poly-Si TFTs," *Solid. State. Electron.*, vol. 43, no. 10, pp. 1821–1831, Oct. 1999, doi: 10.1016/S0038-1101(99)00142-2.

[78] M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack, and B. Iniguez, "Short-channel DC SPICE model for polysilicon thin-film transistors including temperature effects," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1146–1158, 1999, doi: 10.1109/16.766877.

[79] M. J. Siddiqui and S. Qureshi, "Surface-potential-based charge sheet model for the polysilicon thin film transistors without considering kink effect," *Microelectronics J.*, vol. 32, no. 3, pp. 235–240, Mar. 2001, doi: 10.1016/S0026-2692(00)00131-2.

[80] W. J. Wu, R. H. Yao, S. H. Li, Y. F. Hu, W. L. Deng, and X. R. Zheng, "A compact model for polysilicon TFTs leakage current including the Poole-Frenkel effect," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2975–2983, Nov. 2007, doi: 10.1109/TED.2007.906968.

[81] C. Sathe and S. Mahapatra, "Modeling and analysis of noise margin in SET logic," *Proc. IEEE Int. Conf. VLSI Des.*, pp. 207–212, 2007, doi: 10.1109/VLSID.2007.109.

[82] H. H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C. C. Wu, "Modeling of amorphous InGaZn O4 thin film transistors and their subgap density of states," *Appl. Phys. Lett.*, vol. 92, no. 13, Mar. 2008, doi: 10.1063/1.2857463/238046.

[83] L. Li, M. Debucquoy, J. Genoe, and P. Heremans, "A compact model for polycrystalline pentacene thin-film transistor," *J. Appl. Phys.*, vol. 107, no. 2, Jan. 2010, doi: 10.1063/1.3294617/399406.

[84] W. S. Zhao, J. Duval, D. Ravelosona, J. O. Klein, J. V. Kim, and C. Chappert, "A compact model of domain wall propagation for logic and memory design," *J. Appl. Phys.*, vol. 109, no. 7, Apr. 2011, doi: 10.1063/1.3536793/926615.

[85] J. A. J. Tejada, J. A. L. Villanueva, P. L. Varo, K. M. Awawdeh, and M. J. Deen, "Compact modeling and contact effects in thin film transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 266–277, 2014, doi: 10.1109/TED.2013.2282994.

[86] N. Lu, L. Li, and M. Liu, "Universal carrier thermoelectric-transport model based on percolation theory in organic semiconductors," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 91, no. 19, p. 195205, May 2015, doi: 10.1103/PHYSREVB.91.195205/FIGURES/5/THUMBNAIL.

[87] A. Valletta *et al.*, "A compact spice model for organic TFTs and applications to logic circuit design," *IEEE Trans. Nanotechnol.*, vol. 15, no. 5, pp. 754–761, Sep. 2016, doi: 10.1109/TNANO.2016.2542851.

[88] M. Ghittorelli *et al.*, "Physical-based analytical model of flexible a-IGZO TFTs accounting for both charge injection and transport," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2016-February, pp. 28.2.1-28.2.4, Feb. 2015, doi: 10.1109/IEDM.2015.7409786.

[89] W. E. Muhea, T. Gneiting, and B. Iniguez, "UMEM based 1/f noise model for amorphous ESL IGZO TFTs," *Lat. Am. Electron Devices Conf. LAEDC 2019*, May 2019, doi: 10.1109/LAED.2019.8714744.

[90] W. E. Muhea, G. U. Castillo, H. C. Ordonez, T. Gneiting, G. Ghibaudo, and B. Iniguez, "Parameter Extraction and Compact Modeling of 1/f Noise for Amorphous ESL IGZO TFTs," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 407–412, 2020, doi: 10.1109/JEDS.2020.2970177.

[91] H. Cortes-Ordonez *et al.*, "Parameter Extraction and Compact Modeling of OTFTs from 150 K to 350 K," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5685–5692, Dec. 2020, doi: 10.1109/TED.2020.3032082.

[92] S. Jung, Y. Bonnassieux, G. Horowitz, S. Jung, B. Iniguez, and C. H. Kim, "Advances in Compact Modeling of Organic Field-Effect Transistors," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 1404–1415, 2020, doi: 10.1109/JEDS.2020.3020312.

[93] A. Kloes *et al.*, "THM-OTFT: A Complete Physics-Based Verilog-A Compact Model for Short-Channel Organic Thin-Film Transistors," *IEEE J. Electron*

Devices Soc., 2023, doi: 10.1109/JEDS.2023.3294598.

[94] M. Singh Mehrolia, A. Verma, and A. Kumar Singh, "Comparative Analysis of Compact Modeled of Low-Voltage OTFTs on Flexible and Silicon Substrates for the Implementation of Logic Circuits," *IEEE J. Flex. Electron.*, vol. 3, no. 7, pp. 341–347, 2024, doi: 10.1109/JFLEX.2024.3471489.

[95] M. S. Mehrolia, D. Kumar, A. Verma, and A. K. Singh, " Fabrication and Compact Modeling of Low-Voltage Flexible Organic TFT Using Self-Assembly of Conductive Polymer Channel Over High- k PMMA/SrZrO$_{\textit{x}}$ Dielectric ," *IEEE Trans. Electron Devices*, pp. 1–6, Aug. 2024, doi: 10.1109/TED.2024.3442165.

[96] M. S. Mehrolia, D. Kumar, A. K. Singh, and J. S. Rana, "Simulation of CMOS Inverter Circuit and 1-Bit Magnitude Comparator Circuit Utilizing Low-Voltage Flexible TFTs," *2024 IEEE 21st India Counc. Int. Conf. INDICON 2024*, 2024, doi: 10.1109/INDICON63790.2024.10958387.

[97] M. S. Mehrolia, S. Dixit, D. Kumar, A. K. Singh, and S. Kumari, "Utilization of Fully Transparent, Flexible, and Compact Modeled Low Voltage TFT for the Simulation of 2:4 and 3:8 Decoder Circuits," *3rd IEEE Int. Conf. Ind. Electron. Dev. Appl. ICIDeA 2025*, 2025, doi: 10.1109/ICIDEA64800.2025.10963069.

[98] M. S. Mehrolia, S. Dixit, D. Kumar, A. K. Singh, S. Kumari, and J. S. Rana, "Implementation of a 4:1 Multiplexer Using Compact Modeled Flexible and Low Voltage OTFT for Realizing it as a Universal Logic Gate," *3rd IEEE Int. Conf. Device Intell. Comput. Commun. Technol. DICCT 2025*, pp. 7–10, 2025, doi: 10.1109/DICCT64131.2025.10986506.

[99] M. S. Mehrolia, A. Verma, N. K. Chourasia, A. Pandey, and A. K. Singh, "A Proposed Fully Transparent, Flexible, and Compact Modeled Low Voltage TFT for Implementation of Full Adder and Subtractor," *IEEE J. Flex. Electron.*, pp. 1–1, May 2024, doi: 10.1109/JFLEX.2024.3400760.

[100] M. S. Mehrolia, A. K. Mishra, R. Singh, S. Yadav, V. Devarakonda, and A. K. Singh, "Implementation of Digital Logic Gate Families Using Low Operating Flexible Organic TFT Based on Innovative Compact Modeling Approach," *3rd IEEE Int. Conf. Ind. Electron. Dev. Appl. ICIDeA 2025*, 2025, doi:

10.1109/ICIDEA64800.2025.10963231.

[101] M. S. Mehrolia, A. K. Singh, and A. Verma, “A User Guide for Familiarizing with Silvaco-Techmodeler and Silvaco-Gateway Tools,” *Proc. 9th Int. Conf. Commun. Electron. Syst. ICCES 2024*, pp. 147–152, 2024, doi: 10.1109/ICCES63552.2024.10859980.

[102] Y. Kuo, “Thin film transistor technology-Past, present, and future,” *Electrochem. Soc. Interface*, vol. 22, no. 1, pp. 55–61, Jan. 2013, doi: 10.1149/2.F06131IF/XML.

[103] X. Fan *et al.*, “PEDOT:PSS for Flexible and Stretchable Electronics: Modifications, Strategies, and Applications,” *Adv. Sci.*, vol. 6, no. 19, p. 1900813, Oct. 2019, doi: 10.1002/ADVS.201900813.

[104] S. Chung, S. O. Kim, S. K. Kwon, C. Lee, and Y. Hong, “All-inkjet-printed organic thin-film transistor inverter on flexible plastic substrate,” *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1134–1136, Aug. 2011, doi: 10.1109/LED.2011.2156757.

[105] M. E. Roberts, S. C. B. Mannsfeld, R. M. Stoltenberg, and Z. Bao, “Flexible, plastic transistor-based chemical sensors,” *Org. Electron.*, vol. 10, no. 3, pp. 377–383, May 2009, doi: 10.1016/J.ORGEL.2008.12.001.

[106] S. D. Yambem *et al.*, “A highly porous and conductive composite gate electrode for OTFT sensors,” *RSC Adv.*, vol. 9, no. 13, pp. 7278–7284, Mar. 2019, doi: 10.1039/C9RA00148D.

[107] W. Tao, P. Lin, J. Hu, S. Ke, J. Song, and X. Zeng, “A sensitive DNA sensor based on an organic electrochemical transistor using a peptide nucleic acid-modified nanoporous gold gate electrode,” *RSC Adv.*, vol. 7, no. 82, pp. 52118–52124, Nov. 2017, doi: 10.1039/C7RA09832D.

[108] C. W. Shih and A. Chin, “Remarkably High Mobility Thin-Film Transistor on Flexible Substrate by Novel Passivation Material,” *Sci. Rep.*, vol. 7, no. 1, pp. 1–8, Dec. 2017, doi: 10.1038/S41598-017-01231-3;TECHMETA=120,128;SUBJMETA=1005,1007,166,301,639,987;KWRD=ELECTRICAL+AND+ELECTRONIC+ENGINEERING,ELECTRONIC+DEVICES.

[109] D. C. Glass, “A REVIEW OF THE HEALTH EFFECTS OF HYDROGEN SULPHIDE EXPOSURE,” *Ann. Occup. Hyg.*, vol. 34, no. 3, pp. 323–327, Jun. 1990, doi: 10.1093/ANNHYG/34.3.323.

[110] K. H. Kim, E. C. Jeon, Y. J. Choi, and Y. S. Koo, “The emission characteristics and the related malodor intensities of gaseous reduced sulfur compounds (RSC) in a large industrial complex,” *Atmos. Environ.*, vol. 40, no. 24, pp. 4478–4490, Aug. 2006, doi: 10.1016/J.ATMOSENV.2006.04.026.

[111] “HSE: Information about health and safety at work.” https://www.hse.gov.uk/ (accessed Jun. 09, 2025).

[112] F. R. Simões and M. G. Xavier, “Electrochemical Sensors,” *Nanosci. its Appl.*, pp. 155–178, Jan. 2017, doi: 10.1016/B978-0-323-49780-0.00006-5.

[113] S. M. Kanan, O. M. El-Kadri, I. A. Abu-Yousef, and M. C. Kanan, “Semiconducting Metal Oxide Based Sensors for Selective Gas Pollutant Detection,” *Sensors 2009, Vol. 9, Pages 8158-8196*, vol. 9, no. 10, pp. 8158–8196, Oct. 2009, doi: 10.3390/S91008158.

[114] C. Duc, M. L. Boukhenane, J. L. Wojkiewicz, and N. Redon, “Hydrogen Sulfide Detection by Sensors Based on Conductive Polymers: A Review,” *Front. Mater.*, vol. 7, p. 215, Sep. 2020, doi: 10.3389/FMATS.2020.00215/BIBTEX.

[115] M. Shaji, K. J. Saji, and M. K. Jayaraj, “Low temperature operated ZTO thin film transistor based gas sensor for selective detection of H2S,” *Mater. Sci. Semicond. Process.*, vol. 150, p. 106927, Nov. 2022, doi: 10.1016/J.MSSP.2022.106927.

[116] Z. Zeng, K. Wang, Z. Zhang, J. Chen, and W. Zhou, “The detection of H2S at room temperature by using individual indium oxide nanowire transistors,” *Nanotechnology*, vol. 20, no. 4, p. 045503, Dec. 2008, doi: 10.1088/0957-4484/20/4/045503.

[117] N. K. Singh, A. Raman, S. Singh, and N. Kumar, “A novel high mobility In1-xGaxAs cylindrical-gate-nanowire FET for gas sensing application with enhanced sensitivity,” *Superlattices Microstruct.*, vol. 111, pp. 518–528, Nov. 2017, doi: 10.1016/J.SPMI.2017.07.001.

[118] N. Jayaswal, A. Raman, N. Kumar, and S. Singh, “Design and analysis of

electrostatic-charge plasma based dopingless IGZO vertical nanowire FET for ammonia gas sensing," *Superlattices Microstruct.*, vol. 125, pp. 256–270, Jan. 2019, doi: 10.1016/J.SPMI.2018.11.009.

[119] J. T. Mabeck and G. G. Malliaras, "Chemical and biological sensors based on organic thin-film transistors," *Anal. Bioanal. Chem.*, vol. 384, no. 2, pp. 343–353, Jan. 2006, doi: 10.1007/S00216-005-3390-2.

[120] C. Liao and F. Yan, "Organic Semiconductors in Organic Thin-Film Transistor-Based Chemical and Biological Sensors," *https://doi.org/10.1080/15583724.2013.808665*, vol. 53, no. 3, pp. 352–406, Jul. 2013, doi: 10.1080/15583724.2013.808665.

[121] D. Elkington, N. Cooling, W. Belcher, P. C. Dastoor, and X. Zhou, "Organic Thin-Film Transistor (OTFT)-Based Sensors," *Electron. 2014, Vol. 3, Pages 234-254*, vol. 3, no. 2, pp. 234–254, Apr. 2014, doi: 10.3390/ELECTRONICS3020234.

[122] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, "Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer," *J. Phys. Chem. B*, vol. 109, no. 21, pp. 10574–10577, Jun. 2005, doi: 10.1021/JP044318F/ASSET/IMAGES/LARGE/JP044318FF00005.JPEG.

[123] A. Verma, V. N. Mishra, and R. Prakash, "Self-Assembled Au/P3HT, High-k Bilayer Dielectric-Based Solution Processed Low Voltage OTFT for Multiparametric Ammonia Sensor at Room Temperature," *IEEE Trans. Electron Devices*, vol. 70, no. 1, pp. 281–287, Jan. 2023, doi: 10.1109/TED.2022.3224092.

[124] Y. Gong *et al.*, "Solution processable high quality ZrO2 dielectric films for low operation voltage and flexible organic thin film transistor applications," *J. Phys. D. Appl. Phys.*, vol. 51, no. 11, p. 115105, Feb. 2018, doi: 10.1088/1361-6463/AAAC1B.

[125] G. X. Liu *et al.*, "High-performance fully amorphous bilayer metal-oxide thin film transistors using ultra-thin solution-processed ZrOx dielectric," *Appl. Phys. Lett.*, vol. 105, no. 11, p. 113509, Sep. 2014, doi: 10.1063/1.4895782.

[126] M. Houssa *et al.*, “Electrical properties of high-κ gate dielectrics: Challenges, current issues, and possible solutions,” *Mater. Sci. Eng. R Reports*, vol. 51, no. 4–6, pp. 37–85, Apr. 2006, doi: 10.1016/J.MSER.2006.04.001.

[127] B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T. J. Marks, and A. Facchetti, “High- k Gate Dielectrics for Emerging Flexible and Stretchable Electronics,” *Chem. Rev.*, vol. 118, no. 11, pp. 5690–5754, Jun. 2018, doi: 10.1021/ACS.CHEMREV.8B00045/ASSET/IMAGES/LARGE/CR-2018-00045G_0040.JPEG.

[128] M. R. Cavallari *et al.*, “Organic Thin-Film Transistors as Gas Sensors: A Review,” *Mater. 2021, Vol. 14, Page 3*, vol. 14, no. 1, p. 3, Dec. 2020, doi: 10.3390/MA14010003.

[129] N. Tasaltin, D. Sanli, A. Jonáš, A. Kiraz, and C. Erkey, “Preparation and characterization of superhydrophobic surfaces based on hexamethyldisilazane-modified nanoporous alumina,” *Nanoscale Res. Lett.*, vol. 6, no. 1, pp. 1–8, Aug. 2011, doi: 10.1186/1556-276X-6-487/FIGURES/5.

[130] P. K. Sahu *et al.*, “Fast Development of Self-Assembled, Highly Oriented Polymer Thin Film and Observation of Dual Sensing Behavior of Thin Film Transistor for Ammonia Vapor,” *Macromol. Chem. Phys.*, vol. 220, no. 11, p. 1900010, Jun. 2019, doi: 10.1002/MACP.201900010.

[131] A. Verma, P. K. Sahu, V. Chaudhary, A. K. Singh, V. N. Mishra, and R. Prakash, “Fabrication and Characterization of P3HT/MoS Thin-Film Based Ammonia Sensor Operated at Room Temperature,” *IEEE Sens. J.*, vol. 22, no. 11, pp. 10361–10369, Jun. 2022, doi: 10.1109/JSEN.2022.3170698.

[132] W. J. Yoon and P. R. Berger, “Atomic layer deposited HfO2 gate dielectrics for low-voltage operating, high-performance poly-(3-hexythiophene) organic thin-film transistors,” *Org. Electron.*, vol. 11, no. 11, pp. 1719–1722, Nov. 2010, doi: 10.1016/J.ORGEL.2010.07.026.

[133] F. C. Chen, C. S. Chuang, Y. S. Lin, L. J. Kung, T. H. Chen, and H. P. D. Shieh, “Low-voltage organic thin-film transistors with polymeric nanocomposite dielectrics,” *Org. Electron.*, vol. 7, no. 5, pp. 435–439, Oct. 2006, doi: 10.1016/J.ORGEL.2006.06.009.

[134] M. Elsobky *et al.*, “A digital library for a flexible low-voltage organic thin-film transistor technology,” *Org. Electron.*, vol. 50, pp. 491–498, Nov. 2017, doi: 10.1016/J.ORGEL.2017.08.028.

[135] J. Zou *et al.*, “High-k polymer materials containing cyclic carbonate as gate dielectrics for application in low-voltage operating organic thin-film transistors,” *J. Mater. Chem. C*, vol. 7, no. 48, pp. 15357–15363, Dec. 2019, doi: 10.1039/C9TC04417E.

[136] G. D. Tabi, J. S. Kim, B. Nketia-Yawson, D. H. Kim, and Y. Y. Noh, “High-capacitance polyurethane ionogels for low-voltage operated organic transistors and pressure sensors,” *J. Mater. Chem. C*, vol. 8, no. 47, pp. 17107–17113, Dec. 2020, doi: 10.1039/D0TC02364G.

[137] Y. Fujisaki, H. Sato, H. Fujikake, Y. Inoue, S. Tokito, and T. Kurita, “Liquid crystal display cells fabricated on plastic substrate driven by low-voltage organic thin-film transistor with improved gate insulator and passivation layer,” *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap.*, vol. 44, no. 6 A, pp. 3728–3732, Jun. 2005, doi: 10.1143/JJAP.44.3728/XML.

[138] F. Gholamrezaie *et al.*, “Charge Trapping by Self-Assembled Monolayers as the Origin of the Threshold Voltage Shift in Organic Field-Effect Transistors,” *Small*, vol. 8, no. 2, pp. 241–245, Jan. 2012, doi: 10.1002/SMLL.201101467.

[139] B. Nketia-Yawson and Y. Y. Noh, “Organic thin film transistor with conjugated polymers for highly sensitive gas sensors,” *Macromol. Res.*, vol. 25, no. 6, pp. 489–495, Jun. 2017, doi: 10.1007/S13233-017-5108-7/METRICS.

[140] A. M. Andringa *et al.*, “Gas sensing with self-assembled monolayer field-effect transistors,” *Org. Electron.*, vol. 11, no. 5, pp. 895–898, May 2010, doi: 10.1016/J.ORGEL.2010.02.007.

[141] O. Knopfmacher *et al.*, “Highly stable organic polymer field-effect transistor sensor for selective detection in the marine environment,” *Nat. Commun. 2014 51*, vol. 5, no. 1, pp. 1–9, Jan. 2014, doi: 10.1038/ncomms3954.

[142] P. K. Sahu *et al.*, “Air-stable vapor phase sensing of ammonia in sub-threshold regime of poly(2,5-bis(3-tetradecylthiophen-2yl)thieno(3,2-b)thiophene) based polymer thin-film transistor,” *Sensors Actuators B Chem.*, vol. 246, pp. 243–251,

Jul. 2017, doi: 10.1016/J.SNB.2017.02.063.

[143] M. Labed and N. Sengouga, “Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability,” *J. Comput. Electron.*, vol. 18, no. 2, pp. 509–518, 2019, doi: 10.1007/s10825-019-01316-4.

[144] S. Han, X. Zhuang, W. Shi, X. Yang, L. Li, and J. Yu, “Poly(3-hexylthiophene)/polystyrene (P3HT/PS) blends based organic field-effect transistor ammonia gas sensor,” *Sensors Actuators B Chem.*, vol. 225, pp. 10–15, Mar. 2016, doi: 10.1016/J.SNB.2015.11.005.

[145] A. K. Singh, A. Pandey, and P. Chakrabarti, “Poly[2,5-bis(3-tetradecylthiophen-2-yl) thieno [3,2-b] thiophene] Organic Polymer Based-Interdigitated Channel Enabled Thin Film Transistor for Detection of Selective Low ppm Ammonia Sensing at 25°C,” *IEEE Sens. J.*, vol. 20, no. 8, pp. 4047–4055, Apr. 2020, doi: 10.1109/JSEN.2019.2963269.

[146] D. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. Bao, “Humidity effect on electrical performance of organic thin-film transistors,” *Appl. Phys. Lett.*, vol. 86, no. 4, p. 42105, Jan. 2005, doi: 10.1063/1.1852708/117177.

[147] H. W. Zan, W. W. Tsai, Y. R. Lo, Y. M. Wu, and Y. S. Yang, “Pentacene-based organic thin film transistors for ammonia sensing,” *IEEE Sens. J.*, vol. 12, no. 3, pp. 594–601, 2012, doi: 10.1109/JSEN.2011.2121901.

[148] W. H. Tao and C. H. Tsai, “H2S sensing properties of noble metal doped WO3 thin film sensor fabricated by micromachining,” *Sensors Actuators B Chem.*, vol. 81, no. 2–3, pp. 237–247, Jan. 2002, doi: 10.1016/S0925-4005(01)00958-3.

[149] A. Varga, Z. Bozóki, M. Szakáll, and G. Szabó, “Photoacoustic system for on-line process monitoring of hydrogen sulfide (H2S) concentration in natural gas streams,” *Appl. Phys. B Lasers Opt.*, vol. 85, no. 2–3, pp. 315–321, Nov. 2006, doi: 10.1007/S00340-006-2388-6/METRICS.

[150] C. Yu, Y. Wang, K. Hua, W. Xing, and T. Lu, “Electrochemical H2S sensor with H2SO4 pre-treated Nafion membrane as solid polymer electrolyte,” *Sensors Actuators B Chem.*, vol. 86, no. 2–3, pp. 259–265, Sep. 2002, doi: 10.1016/S0925-4005(02)00200-9.

[151] A. A. Trul, V. P. Chekusova, M. S. Polinskaya, A. N. Kiselev, E. V. Agina, and S. A. Ponomarenko, “NH3 and H2S real-time detection in the humid air by two-layer Langmuir-Schaefer OFETs,” *Sensors Actuators B Chem.*, vol. 321, p. 128609, Oct. 2020, doi: 10.1016/J.SNB.2020.128609.

[152] V. K. Singh, A. Verma, P. Kumar, and V. N. Mishra, “Solution-Processed, Highly-Efficient Organic Field-Effect Transistor Based Hydrogen Sulfide Gas Sensor at Sub-ppm Regime,” *IEEE Sens. J.*, vol. 23, no. 15, pp. 16600–16607, Aug. 2023, doi: 10.1109/JSEN.2023.3288932.

[153] O. H. Salinas, C. López-Mata, H. Hu, M. E. Nicho, and A. Sánchez, “Metal contact properties of poly3-octylthiophene thin films,” *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 6, pp. 760–769, Apr. 2006, doi: 10.1016/J.SOLMAT.2005.04.013.

[154] J. Fidyk, W. Waliszewski, P. Sleczkowski, A. Kiersnowski, W. Pisula, and T. Marszalek, “Switching from Electron to Hole Transport in Solution-Processed Organic Blend Field-Effect Transistors,” *Polym. 2020, Vol. 12, Page 2662*, vol. 12, no. 11, p. 2662, Nov. 2020, doi: 10.3390/POLYM12112662.

[155] B. Xu, G. Saianand, V. A. L. Roy, Q. Qiao, K. M. Reza, and S. W. Kang, “Employing PCBTDPP as an Efficient Donor Polymer for High Performance Ternary Polymer Solar Cells,” *Polymers (Basel).*, vol. 11, no. 9, 2019, doi: 10.3390/POLYM11091423.

[156] C. G. Tang *et al.*, “Doped polymer semiconductors with ultrahigh and ultralow work functions for ohmic contacts,” *Nat. 2016 5397630*, vol. 539, no. 7630, pp. 536–540, Nov. 2016, doi: 10.1038/nature20133.

[157] A. Verma, R. Gupta, A. S. Verma, and T. Kumar, “A review of composite conducting polymer-based sensors for detection of industrial waste gases,” *Sensors and Actuators Reports*, vol. 5, p. 100143, Jun. 2023, doi: 10.1016/J.SNR.2023.100143.

[158] X. Fan *et al.*, “PEDOT:PSS for Flexible and Stretchable Electronics: Modifications, Strategies, and Applications,” *Adv. Sci.*, vol. 6, no. 19, p. 1900813, Oct. 2019, doi: 10.1002/ADVS.201900813.

[159] T. Wang, Y. Guo, P. Wan, H. Zhang, X. Chen, and X. Sun, “Flexible Transparent

Electronic Gas Sensors," *Small*, vol. 12, no. 28, pp. 3748–3756, Jul. 2016, doi: 10.1002/SMLL.201601049.

[160] C. S. Luo, P. Wan, H. Yang, S. A. A. Shah, and X. Chen, "Healable Transparent Electronic Devices," *Adv. Funct. Mater.*, vol. 27, no. 23, p. 1606339, Jun. 2017, doi: 10.1002/ADFM.201606339.

[161] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, 2001, doi: 10.1109/5.915374.

[162] W. G. Song *et al.*, "High-Performance Flexible Multilayer MoS2 Transistors on Solution-Based Polyimide Substrates," *Adv. Funct. Mater.*, vol. 26, no. 15, pp. 2426–2434, Apr. 2016, doi: 10.1002/ADFM.201505019.

[163] T. Morita, V. Singh, S. Nagamatsu, S. Oku, W. Takashima, and K. Kaneto, "Enhancement of transport characteristics in poly(3-hexylthiophene) films deposited with floating film transfer method," *Appl. Phys. Express*, vol. 2, no. 11, p. 111502, Nov. 2009, doi: 10.1143/APEX.2.111502/XML.

[164] Y. Fujisaki *et al.*, "Transparent Nanopaper-Based Flexible Organic Thin-Film Transistor Array," *Adv. Funct. Mater.*, vol. 24, no. 12, pp. 1657–1663, Mar. 2014, doi: 10.1002/ADFM.201303024.

[165] D. Khim *et al.*, "Spray-printed organic field-effect transistors and complementary inverters," *J. Mater. Chem. C*, vol. 1, no. 7, pp. 1500–1506, Jan. 2013, doi: 10.1039/C2TC00085G.

[166] U. Pandey, N. Pal, V. Acharya, P. K. Aich, A. K. Yadav, and B. N. Pal, "Dual-Gated Low Operating Voltage Metal Oxide Thin-Film Transistor for Highly Sensitive and Fast-Response Pressure Sensing Application," *IEEE Sens. J.*, vol. 23, no. 11, pp. 11482–11489, Jun. 2023, doi: 10.1109/JSEN.2023.3265992.

[167] U. Pandey, N. K. Chourasia, N. Pal, S. Biring, and B. N. Pal, "Functional Dielectric Properties of Solution-Processed Lithium Indium Tin Oxide (LiInSnO4) and Its Application as a Gate Insulator of a Low Voltage Thin Film Transistor," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1077–1082, Mar. 2022, doi: 10.1109/TED.2022.3147153.

[168] M. S. Mehrolia, D. Kumar, A. Verma, and A. K. Singh, “Fabrication and Characterization of Self-Assembled Low Voltage Operated OTFT for H$_{\text{2}}$S Gas Sensor for Oil and Gas Industry,” *IEEE Trans. Electron Devices*, pp. 1–8, Dec. 2023, doi: 10.1109/TED.2023.3336301.

[169] R. M. Meixner *et al.*, “A physical-based PSPICE compact model for poly(3-hexylthiophene) organic field-effect transistors,” *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1776–1781, Jul. 2008, doi: 10.1109/TED.2008.925339.

[170] A. Valletta *et al.*, “A compact Spice model for organic TFTs and applications to logic circuit design,” *IEEE-NANO 2015 - 15th Int. Conf. Nanotechnol.*, pp. 1434–1437, 2015, doi: 10.1109/NANO.2015.7388909.

[171] C. Kumar, G. Rawat, H. Kumar, Y. Kumar, R. Prakash, and S. Jit, “Electrical and Optical Characteristics of PQT-12-Based Organic TFTs Fabricated by Floating-Film Transfer Method,” *IEEE Trans. Nanotechnol.*, vol. 17, no. 6, pp. 1111–1117, Nov. 2018, doi: 10.1109/TNANO.2018.2846230.

[172] A. Verma, V. N. Mishra, and R. Prakash, “Air-Stable Highly Sensitive Self-Assembled P3HT/GQD nanocomposite based Organic Thin Film Transistor for Multiparametric H_2S Real-time Detection at Room Temperature,” *IEEE Sens. J.*, 2022, doi: 10.1109/JSEN.2022.3221997.

[173] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, “Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer,” *J. Phys. Chem. B*, vol. 109, no. 21, pp. 10574–10577, Jun. 2005, doi: 10.1021/JP044318F/ASSET/IMAGES/LARGE/JP044318FF00005.JPEG.

[174] “Typical Applications TechModeler Modeling Flow • Organic transistors, OLED, solar cells, sensors, memory… Sensors Transistors Memory OLED Photovoltaic Cells STEP 1 Measurements STEP 4 Circit Simulation STEP 2 Model Creations STEP 3 Model Export”.

[175] P. Xie *et al.*, “Solution-processed ultra-flexible C8-BTBT organic thin-film transistors with the corrected mobility over 18 cm2/(V s),” *Sci. Bull.*, vol. 65, no. 10, pp. 791–795, May 2020, doi: 10.1016/J.SCIB.2020.03.013.

[176] B. Yaman, I. Terkesli, K. M. Turksoy, A. Sanyal, and S. Mutlu, “Fabrication of a

planar water gated organic field effect transistor using a hydrophilic polythiophene for improved digital inverter performance," *Org. Electron.*, vol. 15, no. 3, pp. 646–653, Mar. 2014, doi: 10.1016/J.ORGEL.2013.12.024.

[177] D. Khim *et al.*, "Spray-printed organic field-effect transistors and complementary inverters," *J. Mater. Chem. C*, vol. 1, no. 7, pp. 1500–1506, Jan. 2013, doi: 10.1039/C2TC00085G.

[178] T. N. Ng *et al.*, "Electrical stability of inkjet-patterned organic complementary inverters measured in ambient conditions," *Appl. Phys. Lett.*, vol. 94, no. 23, Jun. 2009, doi: 10.1063/1.3153510/337310.

[179] Y. Takeda *et al.*, "Organic Complementary Inverter Circuits Fabricated with Reverse Offset Printing," *Adv. Electron. Mater.*, vol. 4, no. 1, p. 1700313, Jan. 2018, doi: 10.1002/AELM.201700313.

[180] X. He, W. L. Chow, F. Liu, B. K. Tay, and Z. Liu, "MoS2/Rubrene van der Waals Heterostructure: Toward Ambipolar Field-Effect Transistors and Inverter Circuits," *Small*, vol. 13, no. 2, p. 1602558, Jan. 2017, doi: 10.1002/SMLL.201602558.

[181] "Logic Guide," 2017, Accessed: Oct. 12, 2023. [Online]. Available: www.ti.com

[182] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nat. 2004 4327016*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[183] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap.*, vol. 45, no. 5 B, pp. 4303–4308, May 2006, doi: 10.1143/JJAP.45.4303/XML.

[184] J. F. Wager, B. Yeh, R. L. Hoffman, and D. A. Keszler, "An amorphous oxide semiconductor thin-film transistor route to oxide electronics," *Curr. Opin. Solid State Mater. Sci.*, vol. 18, no. 2, pp. 53–61, Apr. 2014, doi: 10.1016/J.COSSMS.2013.07.002.

[185] J. Sheng *et al.*, "Amorphous IGZO TFT with High Mobility of ∼70 cm2/(V s)

via Vertical Dimension Control Using PEALD," *ACS Appl. Mater. Interfaces*, vol. 11, no. 43, pp. 40300–40309, Oct. 2019, doi: 10.1021/ACSAMI.9B14310.

[186] Y. Tang, Y. Song, and K. Nomura, "Long-Term Sustainability of High-Mobility Ultrathin a-IGZO TFT with Double-Layered Passivation," *ACS Appl. Mater. Interfaces*, vol. 17, no. 33, pp. 47170–47179, Aug. 2025, doi: 10.1021/ACSAMI.5C08848.

[187] J. Martins *et al.*, "Bias Stress and Temperature Impact on InGaZnO TFTs and Circuits," *Mater. 2017, Vol. 10, Page 680*, vol. 10, no. 6, p. 680, Jun. 2017, doi: 10.3390/MA10060680.

[188] Y. Shao, X. Wu, M. N. Zhang, W. J. Liu, and S. J. Ding, "High-Performance a-InGaZnO Thin-Film Transistors with Extremely Low Thermal Budget by Using a Hydrogen-Rich Al2O3 Dielectric," *Nanoscale Res. Lett. 2019 141*, vol. 14, no. 1, pp. 122-, Apr. 2019, doi: 10.1186/S11671-019-2959-1.

[189] S. Heo *et al.*, "Origin of positive Vth shift and mobility effects in amorphous GaInZnO thin films," *Thin Solid Films*, vol. 616, pp. 456–460, Oct. 2016, doi: 10.1016/J.TSF.2016.09.005.

[190] K. Domen, T. Miyase, K. Abe, H. Hosono, and T. Kamiya, "Positive-bias stress test on amorphous In-Ga-Zn-O thin film transistor: Annealing-temperature dependence," *IEEE/OSA J. Disp. Technol.*, vol. 10, no. 11, pp. 975–978, Nov. 2014, doi: 10.1109/JDT.2014.2350518.

[191] E. Lee, M. D. H. Chowdhury, M. S. Park, and J. Jang, "Effect of top gate bias on photocurrent and negative bias illumination stress instability in dual gate amorphous indium-gallium-zinc oxide thin-film transistor," *Appl. Phys. Lett.*, vol. 107, no. 23, Dec. 2015, doi: 10.1063/1.4937441/30405.

[192] A. Olziersky *et al.*, "Role of Ga2O3–In2O3–ZnO channel composition on the electrical performance of thin-film transistors," *Mater. Chem. Phys.*, vol. 131, no. 1–2, pp. 512–518, Dec. 2011, doi: 10.1016/J.MATCHEMPHYS.2011.10.013.

[193] K. A. Kim, M. J. Park, W. H. Lee, and S. M. Yoon, "Characterization of negative bias-illumination-stress stability for transparent top-gate In-Ga-Zn-O thin-film transistors with variations in the incorporated oxygen content," *J. Appl. Phys.*, vol. 118, no. 23, Dec. 2015, doi: 10.1063/1.4938013/141665.

[194] E. N. Cho, J. H. Kang, and I. Yun, “Effects of channel thickness variation on bias stress instability of InGaZnO thin-film transistors,” *Microelectron. Reliab.*, vol. 51, no. 9–11, pp. 1792–1795, Sep. 2011, doi: 10.1016/J.MICROREL.2011.07.018.

[195] K. Yamada, K. Nomura, K. Abe, S. Takeda, and H. Hosono, “Examination of the ambient effects on the stability of amorphous indium-gallium-zinc oxide thin film transistors using a laser-glass-sealing technology,” *Appl. Phys. Lett.*, vol. 105, no. 13, Sep. 2014, doi: 10.1063/1.4896948/384913.

[196] C. H. Woo, Y. Y. Kim, B. H. Kong, and H. K. Cho, “Effects of the thickness of the channel layer on the device performance of InGaZnO thin-film-transistors,” *Surf. Coatings Technol.*, vol. 205, no. SUPPL. 1, pp. S168–S171, Dec. 2010, doi: 10.1016/J.SURFCOAT.2010.07.036.

[197] Y. S. Chun, S. Chang, and S. Y. Lee, “Effects of gate insulators on the performance of a-IGZO TFT fabricated at room-temperature,” *Microelectron. Eng.*, vol. 88, no. 7, pp. 1590–1593, Jul. 2011, doi: 10.1016/J.MEE.2011.01.076.

[198] R. Yao *et al.*, “Low-temperature fabrication of sputtered high- k HfO2 gate dielectric for flexible a-IGZO thin film transistors,” *Appl. Phys. Lett.*, vol. 112, no. 10, Mar. 2018, doi: 10.1063/1.5022088/34306.

[199] T. E. Taouririt, A. Meftah, N. Sengouga, M. Adaika, S. Chala, and A. Meftah, “Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium–tin–zinc–oxide thin film transistor (a-ITZO TFT): an analytical survey,” *Nanoscale*, vol. 11, no. 48, pp. 23459–23474, Dec. 2019, doi: 10.1039/C9NR03395E.

[200] T. E. Taouririt, A. Meftah, N. Sengouga, M. Adaika, S. Chala, and A. Meftah, “Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium–tin–zinc–oxide thin film transistor (a-ITZO TFT): an analytical survey,” *Nanoscale*, vol. 11, no. 48, pp. 23459–23474, Dec. 2019, doi: 10.1039/C9NR03395E.

[201] A. Marroun, N. A. Touhami, and T. E. El Hamadi, “Improved IGZO-TFT structure Using High-k Gate Dielectric Materials,” *2019 Int. Conf. Wirel. Technol. Embed. Intell. Syst. WITS 2019*, Apr. 2019, doi:

10.1109/WITS.2019.8723852.

[202] B. He, G. He, L. Zhu, J. Cui, E. Fortunato, and R. Martins, “Electrospun Highly Aligned IGZO Nanofiber Arrays with Low-Thermal-Budget for Challenging Transistor and Integrated Electronics,” *Adv. Funct. Mater.*, vol. 34, no. 6, p. 2310264, Feb. 2024, doi: 10.1002/ADFM.202310264.

[203] Y. Zhang, G. He, L. Wang, W. Wang, X. Xu, and W. Liu, “Ultraviolet-Assisted Low-Thermal-Budget-Driven α-InGaZnO Thin Films for High-Performance Transistors and Logic Circuits,” *ACS Nano*, vol. 16, no. 3, pp. 4961–4971, Mar. 2022, doi: 10.1021/ACSNANO.2C01286/ASSET/IMAGES/LARGE/NN2C01286_0008.JPEG.

[204] M. Mativenga, D. Geng, B. Kim, and J. Jang, “Fully transparent and rollable electronics,” *ACS Appl. Mater. Interfaces*, vol. 7, no. 3, pp. 1578–1585, Jan. 2015, doi: 10.1021/AM506937S/SUPPL_FILE/AM506937S_SI_001.AVI.

[205] S. Park, K. Cho, H. Oh, and S. Kim, “Electrical and mechanical characteristics of fully transparent IZO thin-film transistors on stress-relieving bendable substrates,” *Appl. Phys. Lett.*, vol. 109, no. 14, Oct. 2016, doi: 10.1063/1.4964133/32529.

[206] E. M. C. Fortunato *et al.*, “Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature,” *Adv. Mater.*, vol. 17, no. 5, pp. 590–594, Mar. 2005, doi: 10.1002/ADMA.200400368.

[207] R. P. Singh, M. Khosla, I. Saini, and N. Kumar, “Design and Analysis of IGZO Based Junctionless Thin Film Transistor Using SOI Technology,” *Silicon*, vol. 13, no. 7, pp. 2309–2318, Jul. 2021, doi: 10.1007/S12633-020-00803-9/METRICS.

[208] A. Marroun, N. A. Touhami, T. E. El Hamadi, and M. El Bakkali, “High-Performance Indium–Gallium–Zinc Oxide Thin-Film Transistors Based on Anodic Aluminum Oxide,” *Procedia Manuf.*, vol. 32, pp. 729–733, Jan. 2019, doi: 10.1016/J.PROMFG.2019.02.278.

[209] M. Labed and N. Sengouga, “Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability,” *J. Comput.*

Electron., vol. 18, no. 2, pp. 509–518, Jun. 2019, doi: 10.1007/S10825-019-01316-4/METRICS.

[210] T. C. Fung *et al.*, "Two-dimensional numerical simulation of radio frequency sputter amorphous In-Ga-Zn-O thin-film transistors," *J. Appl. Phys.*, vol. 106, no. 8, Oct. 2009, doi: 10.1063/1.3234400/958368.

[211] M. Adaika, A. Meftah, N. Sengouga, and M. Henini, "Numerical simulation of bias and photo stress on indium–gallium–zinc-oxide thin film transistors," *Vacuum*, vol. 120, pp. 59–67, Oct. 2015, doi: 10.1016/J.VACUUM.2015.04.021.

[212] R. Yao *et al.*, "Low-temperature fabrication of sputtered high- k HfO2 gate dielectric for flexible a-IGZO thin film transistors," *Appl. Phys. Lett.*, vol. 112, no. 10, Mar. 2018, doi: 10.1063/1.5022088/34306.

[213] Y. Park, V. Choong, Y. Gao, B. R. Hsieh, and C. W. Tang, "Work function of indium tin oxide transparent conductor measured by photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 68, no. 19, pp. 2699–2701, May 1996, doi: 10.1063/1.116313.

[214] S. C. Kim, Y. S. Kim, and J. Kanicki, "Density of states of short channel amorphous In-Ga-Zn-O thin-film transistor arrays fabricated using manufacturable processes," *Jpn. J. Appl. Phys.*, vol. 54, no. 5, p. 051101, Apr. 2015, doi: 10.7567/JJAP.54.051101/XML.

[215] T. E. Taouririt, A. Meftah, N. Sengouga, M. Adaika, S. Chala, and A. Meftah, "Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium–tin–zinc–oxide thin film transistor (a-ITZO TFT): an analytical survey," *Nanoscale*, vol. 11, no. 48, pp. 23459–23474, Dec. 2019, doi: 10.1039/C9NR03395E.

[216] M. Kemp, M. Meunier, and C. G. Tannous, "Simulation of the amorphous silicon static induction transistor," *Solid. State. Electron.*, vol. 32, no. 2, pp. 149–157, Feb. 1989, doi: 10.1016/0038-1101(89)90182-2.

[217] Y. Zhang, C. H. Huang, and K. Nomura, "High-mobility wide bandgap amorphous gallium oxide thin-film transistors for NMOS inverters," *Appl. Phys. Rev.*, vol. 11, no. 1, Mar. 2024, doi: 10.1063/5.0159529/3271346.

[218] G. Tsaramirsis *et al.*, “A Modern Approach towards an Industry 4.0 Model: From Driving Technologies to Management,” *J. Sensors*, vol. 2022, 2022, doi: 10.1155/2022/5023011.

[219] T. Erlbacher, “Lateral Power Transistors in Integrated Circuits,” 2014, doi: 10.1007/978-3-319-00500-3.

[220] U. Matebesi, G. Mogosetso, C. K. Lebekwe, N. M. J. Ditshego, W. H. Khoo, and S. M. Sultan, “IGZO TFT versus the MOSFET”.

[221] L. Balogh, “Fundamentals of MOSFET and IGBT Gate Driver Circuits Application Report Fundamentals of MOSFET and IGBT Gate Driver Circuits,” 2017, Accessed: Jun. 19, 2024. [Online]. Available: www.ti.com

[222] B. Yu, Y. Yuan, J. Song, and Y. Taur, “A two-dimensional analytical solution for short-channel effects in nanowire MOSFETs,” *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2357–2362, 2009, doi: 10.1109/TED.2009.2028048.

[223] C. Klingshirn *et al.*, “65 years of ZnO research – old and very recent results,” *Phys. status solidi*, vol. 247, no. 6, pp. 1424–1447, Jun. 2010, doi: 10.1002/PSSB.200983195.

[224] R. P. Singh, M. Khosla, I. Saini, and N. Kumar, “Design and Analysis of IGZO Based Junctionless Thin Film Transistor Using SOI Technology,” *Silicon*, vol. 13, no. 7, pp. 2309–2318, Jul. 2021, doi: 10.1007/S12633-020-00803-9/METRICS.

[225] T. Wang, Y. Guo, P. Wan, H. Zhang, X. Chen, and X. Sun, “Flexible Transparent Electronic Gas Sensors,” *Small*, vol. 12, no. 28, pp. 3748–3756, Jul. 2016, doi: 10.1002/SMLL.201601049.

[226] C. S. Luo, P. Wan, H. Yang, S. A. A. Shah, and X. Chen, “Healable Transparent Electronic Devices,” *Adv. Funct. Mater.*, vol. 27, no. 23, p. 1606339, Jun. 2017, doi: 10.1002/ADFM.201606339.

[227] M. E. Roberts, S. C. B. Mannsfeld, R. M. Stoltenberg, and Z. Bao, “Flexible, plastic transistor-based chemical sensors,” *Org. Electron.*, vol. 10, no. 3, pp. 377–383, May 2009, doi: 10.1016/J.ORGEL.2008.12.001.

[228] W. G. Song *et al.*, “High-Performance Flexible Multilayer MoS2 Transistors on

Solution-Based Polyimide Substrates," *Adv. Funct. Mater.*, vol. 26, no. 15, pp. 2426–2434, Apr. 2016, doi: 10.1002/ADFM.201505019.

[229] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, "Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer," *J. Phys. Chem. B*, vol. 109, no. 21, pp. 10574–10577, Jun. 2005, doi: 10.1021/JP044318F/ASSET/IMAGES/LARGE/JP044318FF00005.JPEG.

[230] H. jin Kwon *et al.*, "Comparison of semiconductor growth and charge transport on hydrophobic polymer dielectrics of organic field-effect transistors: Cytop vs. polystyrene," *Org. Electron.*, vol. 77, p. 105485, Feb. 2020, doi: 10.1016/J.ORGEL.2019.105485.

[231] M. R. Beaulieu, J. K. Baral, N. R. Hendricks, Y. Tang, A. L. Briseño, and J. J. Watkins, "Solution processable high dielectric constant nanocomposites based on zro2 nanoparticles for flexible organic transistors," *ACS Appl. Mater. Interfaces*, vol. 5, no. 24, pp. 13096–13103, Dec. 2013, doi: 10.1021/AM404129U/ASSET/IMAGES/LARGE/AM-2013-04129U_0006.JPEG.

[232] N. K. Chourasia, A. Sharma, V. Acharya, N. Pal, S. Biring, and B. N. Pal, "Solution processed low band gap ion-conducting gate dielectric for low voltage metal oxide transistor," *J. Alloys Compd.*, vol. 777, pp. 1124–1132, Mar. 2019, doi: 10.1016/J.JALLCOM.2018.10.163.

[233] R. Yao *et al.*, "Low-temperature fabrication of sputtered high- k HfO2 gate dielectric for flexible a-IGZO thin film transistors," *Appl. Phys. Lett.*, vol. 112, no. 10, Mar. 2018, doi: 10.1063/1.5022088/34306.

[234] N. K. Chourasia, A. Sharma, N. Pal, S. Biring, and B. N. Pal, "Dielectric/Semiconductor Interfacial p-Doping: A New Technique to Fabricate Solution-Processed High-Performance 1 V Ambipolar Oxide Transistors," *Phys. status solidi – Rapid Res. Lett.*, vol. 14, no. 10, p. 2000268, Oct. 2020, doi: 10.1002/PSSR.202000268.

[235] M. S. Mehrolia, A. Verma, N. K. Chourasia, A. Pandey, and A. K. Singh, "A Proposed Fully Transparent, Flexible, and Compact Modeled Low Voltage TFT

for Implementation of Full Adder and Subtractor," *IEEE J. Flex. Electron.*, pp. 1–1, May 2024, doi: 10.1109/JFLEX.2024.3400760.

[236] T. E. Taouririt, A. Meftah, N. Sengouga, M. Adaika, S. Chala, and A. Meftah, "Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium–tin–zinc–oxide thin film transistor (a-ITZO TFT): an analytical survey," *Nanoscale*, vol. 11, no. 48, pp. 23459–23474, Dec. 2019, doi: 10.1039/C9NR03395E.

[237] A. Verma, S. Gupta, V. N. Mishra, and R. Prakash, "A Low-Voltage, Self-Oriented Organic Polymer Nanocomposite-Based Flexible TFT for Ammonia Gas Sensing at Room Temperature," *IEEE Trans. Electron Devices*, vol. 70, no. 5, pp. 2453–2459, May 2023, doi: 10.1109/TED.2023.3255835.

[238] N. Jain, S. K. Sharma, R. Kumawat, A. Jain, and S. Lakhawat, "Influence of high-k dielectric material on the electrical performance of a-IGZO Thin Film Transistor," *Mater. Today Proc.*, vol. 66, pp. 3553–3558, Jan. 2022, doi: 10.1016/J.MATPR.2022.07.013.

[239] M. Labed and N. Sengouga, "Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability," *J. Comput. Electron.*, vol. 18, no. 2, pp. 509–518, Jun. 2019, doi: 10.1007/S10825-019-01316-4/METRICS.

[240] M. Singh Mehrolia, A. Verma, and A. Kumar Singh, "Comparative Analysis of Compact Modeled of Low-Voltage OTFTs on Flexible and Silicon Substrates for the Implementation of Logic Circuits," *IEEE J. Flex. Electron.*, vol. 3, no. 7, pp. 341–347, Jul. 2024, doi: 10.1109/JFLEX.2024.3471489.

[241] A. Sharma, R. Singh, and P. Kajla, "Area Efficient 1-Bit Comparator Design by using Hybridized Full Adder Module based on PTL and GDI Logic," *Int. J. Comput. Appl.*, vol. 82, no. 10, pp. 975–8887, 2013.

[242] M. Aggarwal, M. E. Student, and R. Mehra, "Performance Analysis of Magnitude Comparator using Different Design Techniques," *Int. J. Comput. Appl.*, vol. 115, no. 14, pp. 975–8887, 2015.

[243] A. Sharma, R. Singh, P. K.-I. J. of Computer, and undefined 2013, "Area efficient 1-bit comparator design by using hybridized full adder module based on

PTL and GDI logic," *Acad. Sharma, R Singh, P KajlaInternational J. Comput. Appl. 2013•academia.edu*, Accessed: Aug. 31, 2024. [Online]. Available: https://www.academia.edu/download/79749630/pxc3892316.pdf

[244] M. Aggarwal, R. M.-I. J. of Computer, and undefined 2015, "Performance analysis of magnitude comparator using different design techniques," *Res. Aggarwal, R MehraInternational J. Comput. Appl. 2015•researchgate.net*, vol. 115, no. 14, pp. 975–8887, 2015, doi: 10.5120/20218-2496.

[245] J. Kim, H. Y.-2007 I. A. S.-S. Circuits, and undefined 2007, "Bitwise competition logic for compact digital comparator," *ieeexplore.ieee.orgJY Kim, HJ Yoo2007 IEEE Asian Solid-State Circuits Conf. 2007•ieeexplore.ieee.org*, Accessed: Aug. 31, 2024. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/4425682/

[246] J. E. ANU and R. MANJITH, "DESIGN OF LOW POWER HIGH SPEED HYBRID ADDER," *i-manager's J. Digit. Signal Process.*, vol. 9, no. 2, p. 8, 2021, doi: 10.26634/JDP.9.2.16284.

[247] L. E. M. Brackenbury, "Multiplexer as a universal computing element for electro-optic logic systems," *IEE Proc. J*, vol. 137, no. 5, pp. 305–310, 1990, doi: 10.1049/IP-J.1990.0051.

[248] C. Udhayakumar, … M. N.-I. J. of, and undefined 2014, "Design of various Logic gates and Multiplexer in QCA," *Acad. Udhayakumar, MI Niranjana, R Gowrimanohari, EA KumarInternational J. Adv. Eng. Res. Technol. 2014•academia.edu*, Accessed: Oct. 17, 2024. [Online]. Available: https://www.academia.edu/download/92030066/131116.pdf

[249] K. I. Shohail, W. Awsaf, S. U. Sayel, M. Khanam Nitu, and M. Haque Bhuyan, "Design Steps, Simulation, and Analysis of a 1-bit ALU in Cadence at 90 nm CMOS Node," *IOSR J. VLSI Signal Process. (IOSR-JVSP*, vol. 13, no. 6, pp. 1–14, doi: 10.9790/4200-1306010114.

[250] P. Kuncha, C. Swapna, K. Prathyusha, M. C. Suman, and K. Charan Teja, "DESIGN AND COMPARISION OF A 1-BIT ALU PERFORMANCE USING UNIVERSAL GATES," *Artic. J. Adv. Res. Dyn. Control Syst.*, vol. 9, 2017, Accessed: May 18, 2024. [Online]. Available:

https://www.researchgate.net/publication/322150899

[251] G. J. Lee, J. Kim, J. H. Kim, S. M. Jeong, J. E. Jang, and J. Jeong, “High performance, transparent a-IGZO TFTs on a flexible thin glass substrate,” *Semicond. Sci. Technol.*, vol. 29, no. 3, p. 035003, Jan. 2014, doi: 10.1088/0268-1242/29/3/035003.

[252] T. Kamiya, K. Nomura, and H. Hosono, “Present status of amorphous In–Ga–Zn–O thin-film transistors,” *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, p. 044305, Sep. 2010, doi: 10.1088/1468-6996/11/4/044305.

[253] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nat. 2004 4327016*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[254] J. Y. Kim, N. K. Tak, J. H. Choi, W. S. Lee, W. J. Cho, and J. T. Park, “P-15: Prediction Method of Device Instability in a-InGaZnO TFTs under Positive Gate Biases and Thermal Stresses using TCAD Simulation,” *SID Symp. Dig. Tech. Pap.*, vol. 48, no. 1, pp. 1280–1283, May 2017, doi: 10.1002/SDTP.11869.

[255] Y. J. Chen, Y. H. Tai, and C. Y. Chang, “Mechanism of Hysteresis for a-IGZO TFT Studied by Changing the Gate Voltage Waveform in Measurement,” *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1565–1571, Apr. 2016, doi: 10.1109/TED.2016.2532465.

[256] I.-T. Cho, J.-M. Lee, J.-H. Lee, and H.-I. Kwon, “Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses,” *Semicond. Sci. Technol.*, vol. 24, no. 1, p. 015013, Dec. 2008, doi: 10.1088/0268-1242/24/1/015013.

[257] J. Y. Kim, N. K. Tak, J. H. Choi, W. S. Lee, W. J. Cho, and J. T. Park, “Prediction Method of Device Instability in a-lnGaZnO TFTs under Positive Gate Biases and Thermal Stresses using TCAD Simulation,” *Dig. Tech. Pap. - SID Int. Symp.*, vol. 48, no. 1, pp. 1280–1283, May 2017, doi: 10.1002/SDTP.11869;PAGE:STRING:ARTICLE/CHAPTER.

[258] C. F. Hu, T. Teng, and X. P. Qu, “Two-step degradation of a-InGaZnO thin film transistors under DC bias stress,” *Solid. State. Electron.*, vol. 152, pp. 4–10, Feb.

2019, doi: 10.1016/J.SSE.2018.11.005.

[259] J. I. Kim *et al.*, “Effect of temperature and electric field on degradation in amorphous InGaZnO TFTs under positive gate and drain bias stress,” *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 458–460, 2014, doi: 10.1109/LED.2014.2306818.

[260] S. Choi *et al.*, “Positive Bias Stress Instability of InGaZnO TFTs with Self-Aligned Top-Gate Structure in the Threshold-Voltage Compensated Pixel,” *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 50–53, Jan. 2020, doi: 10.1109/LED.2019.2954543.

[261] Y. D. Kim *et al.*, “Electrical stability analysis of dynamic logic using amorphous indium-gallium-zinc-Oxide TFTs,” *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1128–1131, Jul. 2019, doi: 10.1109/LED.2019.2920634.

[262] M. Mativenga, S. Hong, and J. Jang, “High current stress effects in amorphous-InGaZnO4 thin-film transistors,” *Appl. Phys. Lett.*, vol. 102, no. 2, Jan. 2013, doi: 10.1063/1.4775694/975512.

[263] M. Chun, J. G. Um, M. S. Park, M. D. H. Chowdhury, and J. Jang, “Effect of top gate potential on bias-stress for dual gate amorphous indium-gallium-zinc-oxide thin film transistor,” *AIP Adv.*, vol. 6, no. 7, Jul. 2016, doi: 10.1063/1.4960014/564959.

[264] H. young Jeong, S. hee Nam, K. shik Park, H. chul Choi, and J. Jang, “Finding the cause of degradation of low-temperature oxide thin-film transistors,” *J. Korean Phys. Soc.*, vol. 78, no. 4, pp. 284–289, Feb. 2021, doi: 10.1007/S40042-021-00069-3/FIGURES/6.

[265] H. Liu *et al.*, “High Performance and Hysteresis-Free a-IGZO Thin Film Transistors Based on Spin-Coated Hafnium Oxide Gate Dielectrics,” *IEEE Electron Device Lett.*, vol. 44, no. 9, pp. 1508–1511, Sep. 2023, doi: 10.1109/LED.2023.3295594.

[266] M. M. Billah *et al.*, “Analysis of Improved Performance under Negative Bias Illumination Stress of Dual Gate Driving a-IGZO TFT by TCAD Simulation,” *IEEE Electron Device Lett.*, vol. 37, no. 6, pp. 735–738, Jun. 2016, doi: 10.1109/LED.2016.2557358.

[267] Y. H. Chang, M. J. Yu, R. P. Lin, C. P. Hsu, and T. H. Hou, “Abnormal positive bias stress instability of In-Ga-Zn-O thin-film transistors with low-temperature Al2O3 gate dielectric,” *Appl. Phys. Lett.*, vol. 108, no. 3, Jan. 2016, doi: 10.1063/1.4939905/31431.

[268] M. E. Lopes *et al.*, “Gate-bias stress in amorphous oxide semiconductors thin-film transistors,” *Appl. Phys. Lett.*, vol. 95, no. 6, Aug. 2009, doi: 10.1063/1.3187532/338225.

[269] M. D. H. Chowdhury, P. Migliorato, and J. Jang, “Time-temperature dependence of positive gate bias stress and recovery in amorphous indium-gallium-zinc-oxide thin-film-transistors,” *Appl. Phys. Lett.*, vol. 98, no. 15, Apr. 2011, doi: 10.1063/1.3580611/340354.

[270] C. A. Lee *et al.*, “Hysteresis mechanism in pentacene thin-film transistors with poly(4-vinyl phenol) gate insulator,” *Appl. Phys. Lett.*, vol. 89, no. 26, Dec. 2006, doi: 10.1063/1.2425042/332431.

[271] Z. Yang, J. Yang, T. Meng, M. Qu, and Q. Zhang, “Influence of channel layer thickness on the stability of amorphous indium zinc oxide thin film transistors,” *Mater. Lett.*, vol. 166, pp. 46–50, Mar. 2016, doi: 10.1016/J.MATLET.2015.12.029.

[272] E. N. Cho, J. H. Kang, and I. Yun, “Effects of channel thickness variation on bias stress instability of InGaZnO thin-film transistors,” *Microelectron. Reliab.*, vol. 51, no. 9–11, pp. 1792–1795, Sep. 2011, doi: 10.1016/J.MICROREL.2011.07.018.

[273] Y. S. Chun, S. Chang, and S. Y. Lee, “Effects of gate insulators on the performance of a-IGZO TFT fabricated at room-temperature,” *Microelectron. Eng.*, vol. 88, no. 7, pp. 1590–1593, Jul. 2011, doi: 10.1016/J.MEE.2011.01.076.

[274] J. S. Lee, S. Chang, S. M. Koo, and S. Y. Lee, “High-performance a-IGZO TFT with ZrO2 gate dielectric fabricated at room temperature,” *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 225–227, Mar. 2010, doi: 10.1109/LED.2009.2038806.

[275] P. Ma *et al.*, “Low voltage operation of IGZO thin film transistors enabled by ultrathin Al2O3 gate dielectric,” *Appl. Phys. Lett.*, vol. 112, no. 2, Jan. 2018, doi: 10.1063/1.5003662/986331.

[276] D. H. Kim, H. S. Cha, H. S. Jeong, S. H. Hwang, and H. I. Kwon, “Effects of Active Layer Thickness on the Electrical Characteristics and Stability of High-Mobility Amorphous Indium–Gallium–Tin Oxide Thin-Film Transistors,” *Electron. 2021, Vol. 10, Page 1295*, vol. 10, no. 11, p. 1295, May 2021, doi: 10.3390/ELECTRONICS10111295.

[277] Z. Yang, J. Yang, T. Meng, M. Qu, and Q. Zhang, “Influence of channel layer thickness on the stability of amorphous indium zinc oxide thin film transistors,” *Mater. Lett.*, vol. 166, pp. 46–50, Mar. 2016, doi: 10.1016/J.MATLET.2015.12.029.

[278] M. Labed and N. Sengouga, “Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability,” *J. Comput. Electron.*, vol. 18, no. 2, pp. 509–518, Jun. 2019, doi: 10.1007/S10825-019-01316-4/FIGURES/10.

LIST OF PUBLICATIONS

Journal Publications

1. **M. Singh Mehrolia**, D. Kumar, A. Verma and A. K. Singh, "Fabrication and Characterization of Self-Assembled Low Voltage Operated OTFT for H2S Gas Sensor for Oil and Gas Industry," in *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 769-776, Jan. 2024, doi: 10.1109/TED.2023.3336301.

2. **M. Singh Mehrolia**, D. Kumar, A. Verma and A. Kumar Singh, "Fabrication and Compact Modeling of Low-Voltage Flexible Organic TFT Using Self-Assembly of Conductive Polymer Channel Over High-k PMMA/$SrZrO_x$ Dielectric," in *IEEE Transactions on Electron Devices*, vol. 71, no. 10, pp. 6055-6060, Oct. 2024, doi: 10.1109/TED.2024.3442165.

3. **M. Singh Mehrolia**, A. Verma, A. Kumar Singh, N. K. Chourasia and A. Pandey, "A Proposed Fully Transparent, Flexible, and Compact Modeled Low-Voltage TFT for Implementation of Full Adder and Subtractor," in *IEEE Journal on Flexible Electronics*, vol. 3, no. 11, pp. 477-483, Nov. 2024, doi: 10.1109/JFLEX.2024.3400760.

4. **M. Singh Mehrolia**, A. Verma and A. Kumar Singh, "Comparative Analysis of Compact Modeled of Low-Voltage OTFTs on Flexible and Silicon Substrates for the Implementation of Logic Circuits," in *IEEE Journal on Flexible Electronics*, vol. 3, no. 7, pp. 341-347, July 2024, doi: 10.1109/JFLEX.2024.3471489.

5. **M. Singh Mehrolia**, A. Verma and A. Kumar Singh, “Comprehensive Stability Analysis of Fully Transparent Low-Power Thin-Film Transistors: Role of Device Design and Electrical Parameters” in *IEEE Journal on Flexible Electronics*, doi: 10.1109/JFLEX.2025.3611884.

Conference Publications

1. **M. S. Mehrolia**, A. K. Singh and A. Verma, "A User Guide for Familiarizing with Silvaco-Techmodeler and Silvaco-Gateway Tools," *2024 9th International Conference on Communication and Electronics Systems (ICCES)*, Coimbatore, India, 2024, pp. 147-152, doi: 10.1109/ICCES63552.2024.10859980.
2. **M. S. Mehrolia**, D. Kumar, A. K. Singh and J. S. Rana, "Simulation of CMOS Inverter Circuit and 1-Bit Magnitude Comparator Circuit Utilizing Low-Voltage Flexible TFTs," *2024 IEEE 21st India Council International Conference (INDICON)*, Kharagpur, India, 2024, pp. 1-6, doi: 10.1109/INDICON63790.2024.10958387.
3. **M. S. Mehrolia**, A. K. Mishra, R. Singh, S. Yadav, V. Devarakonda and A. K. Singh, "Implementation of Digital Logic Gate Families Using Low Operating Flexible Organic TFT Based on Innovative Compact Modeling Approach," *2025 3rd IEEE International Conference on Industrial Electronics: Developments & Applications (ICIDeA)*, Bhubaneswar, India, 2025, pp. 1-5, doi: 10.1109/ICIDeA64800.2025.10963231.
4. **M. S. Mehrolia**, S. Dixit, D. Kumar, A. K. Singh and S. Kumari, "Utilization of Fully Transparent, Flexible, and Compact Modeled Low Voltage TFT for the Simulation of 2:4 and 3:8 Decoder Circuits," *2025 3rd IEEE International Conference on Industrial Electronics: Developments & Applications (ICIDeA)*, Bhubaneswar, India, 2025, pp. 1-6, doi: 10.1109/ICIDeA64800.2025.10963069.
5. **M. S. Mehrolia**, S. Dixit, D. Kumar, A. K. Singh, S. Kumari and J. S. Rana, "Implementation of a 4:1 Multiplexer Using Compact Modeled Flexible and Low Voltage OTFT for Realizing it as a Universal Logic Gate," *2025 3rd International Conference on Device Intelligence, Computing and Communication Technologies (DICCT)*, Dehradun, India, 2025, pp. 7-10, doi: 10.1109/DICCT64131.2025.10986506.